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(71) Applicant: LUCENT TECHNOLOGIES INC.
Murray Hill, New Jersey 07974-0636 (US)

(72) Inventors:
- Dittrich, Andreas
67729 Sippersfeld (DE)
- Urbansky, Ralph Steffen, Prof. Dr.
Kaiserslautern 67663 (DE)
- Sauer-Gerff, Wolfgang Emil, Dr.
67661 Kaiserslautern (DE)

(74) Representative: Williams, David John et al
Page White & Farrer,
54 Doughty Street
London WC1N 2LS (GB)

(54) Channel estimation using a probability mapping table

(57) The invention relates to an estimation apparatus of a receiving device for estimating the transmission operation of a transmission channel, in which case the transmission channel is subject to interference, and in which the analogue data (5) received from the transmission channel is assigned an estimator sequence (â) of digital data values, in which the estimator apparatus produces at least one estimation sequence (â), in which both characteristics of the transmission channel and characteristics of the receiver are included, in order in this way to improve the reception characteristics in general and, in particular, the bit error rate of the estimation sequence (â).

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Description

[0001] The invention relates to an estimation apparatus for estimating the transmission operation of a transmission channel for digital data, in which case the transmission channel is or may be subject to interference, and to a receiver and a system for transmitting data using such an estimation apparatus.

[0002] Optical long-distance communications systems with transmission rates of 10 Gbit/s or more and which use standard monomode optical fibres, erbium-doped fibre amplifiers and noncoherent optical receivers, are adversely affected by nonlinear pulse dispersion and signal-dependent non-Gaussian noise. If receiver circuits corresponding to the prior art are used here, losses occur with regard to the range, the data rate or the error rate. This is caused by the square-function characteristic of the optical/electrical transducer and a number of physical phenomena such as chromatic dispersion, polarization-mode dispersion, the nonlinear Kerr effect, chirp, extinction ratio, self-phase modulation or noise resulting from spontaneous emission, see, for example, Agrawal, G.P. in Fiber-Optic Communication Systems. Second Edition, New York: John Wiley & Sons, Inc., 1997.

[0003] The wide range of effects, some of which vary with time, leads on the one hand to the impossibility of producing a closed a priori description of the behaviour of the resultant electrical channel and of the resultant noise. On the other, this results in a nonlinear transmission channel which varies with time and is subject to memory and which has signal-dependent noise with an unknown likelihood density, which must be estimated while data transmission is taking place.

[0004] In addition, problems occur in the provision of suitable receiver circuits for data rates of 10 Gbit/s or more. Furthermore, some digital devices operate in such a way that an analog/digital transducer (ADC) is required for these sampling frequencies. Such components are not prior art and at the moment can be produced only if very poor resolution is accepted, with further static and dynamic nonilinearities, that is to say nonlinearities which are dependent on previous samples.

[0005] Since virtually distortion-free transmission can be assumed at data rates of less than 2.5 Gbit/s in optical long-distance systems, receiver circuits comprising a low-pass filter, automatic gain control and a threshold-value decision maker are regarded as prior art, by means of which the required bit error rate of less than 10^{-12} is achieved. If the data rate on these optical paths is increased, then, however, such arrangements do not take account of the pulse dispersion effects described initially and which now occur. The error rate can then well exceed the permissible limit, depending on a large number of influences, as a result of which the connection will fail at times or entirely. Alternatively, error-correcting coding would have to be provided, with the usable data rate thus being reduced or the distance being shortened.

[0006] Furthermore, approaches are known for compensating for some of the effects by means of optical equalizers, see Heismann, F. et al. in Automatic Compensation of First-Order Polarization Mode Dispersion in a 10 Gb/s Transmission System. Proc. of ECOC'98, pages 529-530, Madrid, 1998. A first disadvantage is that the active optical components required to do this represent a considerable cost factor and, secondly, the signal-theory causes of the problems resulting from this can be only partially solved, and only in comparatively good conditions. The latter also applies to the adaptive electrical filter approach (linear feed forward equalizer). This is because, firstly, this generally increases the noise level and, secondly, it can remove distortion only from linear channels or, in some cases, slightly nonlinear channels.

[0007] The structure of the decision feedback amplifier which is known from Kasturia, S., Winters, J.H. in Techniques for High-Speed Implementation of Nonlinear Cancellation. IEEE Journal on Selected Areas in Communications, Vol. 9, pages 711-717, 1991, is also used for this purpose. This interference compensation principle is, however, fundamentally lossy, and leads to error propagation. Furthermore, the achievable error rate is always dependent on the decision time within the bit interval.

[0008] The theory behind the receiver for nonlinear channels with memory, which makes decisions on the basis of minimum error likelihood, is discussed in the literature, see Benedetto, S., Biglieri E., Castellani, V. in Digital Transmission Theory, New Jersey, Prentice-Hall, 1987. This solution approach relates to a probabilistic estimator for the transmitted bit sequence, which requires a priori knowledge of the signal forms of the nonlinear channel not subject to interference, as well as the conditional likelihoods of the interference. The above statements have shown, however, that neither is known.

[0009] With regard to analogue/digital transducers, known arrangements already exist which comprise a nonlinear instantaneous function, the ADC and a digital correction apparatus, see DE 44 09 063 C1. Since these arrangements are used only to compensate for static effects (for example to increase the drive range), the reaction to dynamic changes of channel characteristics or interference is extremely unsatisfactory. Furthermore, such systems require a fast ADC which, as a result of the problems explained, leads to a further adverse effect on the resultant transmission channel.

[0010] The invention is based on the object of reducing the problems described above and, in particular, of providing an improved estimation apparatus for estimating the transmission operation of a transmission channel for digital data which is subject to inference, as well as a receiver and a system for transmitting data using such an estimation apparatus.

[0011] This object is achieved by an estimation apparatus having the features of Claim 1, by a receiver having the feature of Claim 12, and by a system for transmitting data having the features of Claim 14.

[0012] In a particularly advantageous manner, the estimation apparatus according to the invention is used to produce at least one estimation sequence which includes characteristics not only of the transmission channel but also of the conversion device, and this results in an improvement in the bit error rate of the overall transmission path comprising the transmission channel and the receiving device.

[0013] It is furthermore advantageous to digital/analogue convert the analogue input signal and to assign a value set from a metrics table to the digital/analogue converted value since, in this case, random influences occurring on the transmission path can be taken into account using the values from the metrics table.

[0014] Those effects of the transmission path which are subject to memory can, furthermore, be taken into account in a manner which is efficient in terms of computation, if the values of the metrics table in each case comprise the logarithm of the conditional likelihoods for the possible channel states, which results from a finite number of most recently transmitted symbols.

[0015] In one particularly preferred embodiment, the values in the metrics table become the conditional likelihoods, which in each case cover the likelihood of the occurrence of a received value, subject to the condition that the channel is in a specific state, and with this conditional likelihood being obtained by counting the received subsequent values from the estimation sequence of estimated channel states.

[0016] In one advantageous embodiment, a state in each case corresponds to a digital interval of the digital/analogue transducer, and an element in the metrics table corresponds to the logarithm of the conditional likelihood. In consequence, multiplication operations of likelihoods, which are advantageous in terms of data processing, can be expressed as the addition of their metrics values.

[0017] Major advantages result if the conditional likelihoods are obtained by counting the events in that a received value occurs when the channel is in a state which is obtained from the estimation sequence (â) since, in this case, even a simple memory module can store these values as matrix elements or, in processed form, as elements in a metrics table. Furthermore, if, after completion of a measurement interval, the likelihood is normalized by forming the ratio with the total number of received values which have occurred for each channel state, the pure numerical values obtained in this way themselves represent the respective conditional likelihoods.

[0018] Dynamic adaptation is advantageously made possible by the elements in the metrics table being updated on the basis of the received value sequences.

[0019] This concept can be advantageously implemented by means of a data'estimator to which the associated value set from the metrics table is supplied and which in each case assigns a most likely value of an estimation sequence to the supplied value set and supplies an output signal to a discrete channel estimator which signal describes the estimated channel state.

[0020] In this case, the output signals can advantageously be used for continuous calculation of the metrics table values in the discrete channel estimator, on the basis of histogram values of the conditional likelihoods.

[0021] If the time correlations of those elements of interference or nonlinear effects which are subject to memory act for a longer time than the duration of only one transmitted symbol, the metrics table values may each be associated with more than one previous state change, in this case resulting in corresponding multiplication of the matrix elements of the numerical values and of the elements in the metrics table. In this context, reference is also made to the article by A. Kavcic, J. Moura, The Viterbi Algorithm and Markov Noise Memory, IEEE Trans. Information Theory, Vol. 46, No. 1, Jan. 2000 pp. 291-300 whose contents are incorporated completely here by reference.

[0022] The invention will be described in more detail in the following text using the attached drawings and with reference to preferred embodiments.

Brief description of the figures

[0023]

Figure 1	shows a typical optical transmission path in which the invention can be used,
Figure 2	shows an eye diagram of a signal received from an optical transmission path essentially without any interference, in particular the transmission path shown in Figure 1,
Figures 3a and b	show the comparison of the electrical implementation of a conventional detector and of the receiver structure according to the invention,
Figure 4	shows the quantization characteristic of a quantizer, in particular of an analogue/digital transducer (ADC),
Figure 5	shows a block diagram of the assemblies of the receiver structure from Figure 3b,
Figure 6	shows the transition from numerical values of the respective conditional likelihoods for a quantized or, in particular, digital value for an estimated channel state to metrics values which indicate,

in particular, the logarithm of the respective conditional likelihood,

Figure 7 shows the relationship between the likelihood density function and the likelihood distribution of the quantized or digitized signal.

Detailed description of preferred embodiments

[0024] In the simplest case, an optical transmission system comprises three basic units (illustrated by way of example in Figure 1), a transmitter 1, a transmission medium 2 and a receiver 3. A semiconductor laser whose light intensity is modulated with an electrical signal is preferably used for the transmitter 1.

[0025] Various types of optical fibre may be used as the transmission medium 2, in particular such as monomode fibres, gradient fibres and the like, which allow propagation guided in the form of waveguides for the electromagnetic waves. Commercial systems normally use photodiodes for detection of the optical signals, and these supply a current which is largely proportional to the optical power.

[0026] The task of subsequent detectors is, in general, to reconstruct the original digital data stream 4 with as few errors as possible from the electrical signal 5.

[0027] By way of example, Figure 2 shows the electrical received signals 5, in each case shifted by an integer multiple of a bit interval T and superimposed, of a typical optical transmission path (eye diagram).

[0028] In conventional systems, the electrical signal 5 is sampled at equidistant intervals, corresponding to one bit interval, and is supplied to a simple threshold-value decision maker 6, illustrated by way of example in Figure 3a. A "1" or a "0" is detected as part of a signal sequence â depending on whether the signal is above or below the decision threshold at the sampling time.

[0029] The invention is based on the new receiver structure described in the following text and illustrated by way of example in Figure 3b.

[0030] While conventional detectors, as illustrated in Figure 3a, essentially comprise only a low-pass filter 7 and a threshold-value decision maker 6, together with a device for samples 8 taken at discrete times, the estimation apparatus 9 according to the invention provides a receiver structure with time quantization by means of the sampler 8 and value quantization by means of a quantizer 10, in particular an A/D transducer 10 and a downstream data estimation apparatus 11.

[0031] The electrically preprocessed signal 5 received by the photodiode 3 is supplied to a filter 12 and is sampled by the sampler 8 in time with the symbols. The continuous analogue signal downstream from the filter 12 is converted into a digital signal by means of the analogue/digital transducer 10. The output of the A/D transducer 10 supplies the data estimation apparatus 11 with a discrete value from a set of a finite number of quantized or digitized values, which are associated with the occurrence-of a specific event, for example as the event 1: "the sampled value is between threshold 4- and 5".

[0032] The estimation apparatus according to the invention now tries to reconstruct the transmitted bit sequence 4 as well as possible from the sampled and quantized values.

[0033] This object has been achieved by inventing an estimation apparatus which also includes an estimation device for channel estimation 13, see for example Figure 5, which, on the basis of information arriving from the A/D transducer 10, adaptively adjusts itself to any desired nonlinear channels, non-Gaussian interference and the natural characteristics of the A/D transducer 10 or other imperfections, and compensates for or corrects them as far as possible, and, in particular in conjunction with the estimated channel, carries out an estimation of the transmitted bit sequence 4 in such a manner that the error likelihood in the estimation sequence â is as small as possible.

[0034] The invention thus covers two of the previously mentioned problem areas: firstly, static nonlinearities and dynamic nonlinearities which are dependent on the bit sequence from the A/D transducer 10 are taken into account and thus compensated for. Secondly, both the resultant conditional inference likelihood densities, which are dependent on the bit sequence, and the nonlinear channel model for the probabilistic sequence estimator, are estimated including any required unique characteristic, which is necessarily known, of the A/D transducer while data transmission is taking place.

[0035] Based on the simple model of a quantizer which, in this case, is also regarded as the most general form of a digitizer or A/D transducer, one important aspect of the present estimation apparatus will be explained in more detail in the following text.

[0036] The quantizer provides a function which assigns elements in a finite set to the continuous, real input values. If r denotes the input value and ? denotes the output value of the quantizer, then

Equation 1 $$Q : r \in R \rightarrow Q(r) = \tilde{r} \in \{\tilde{r}^{(1)}, \tilde{r}^{(2)}, \ldots, \tilde{r}^{(p)}\}$$

[0037] Each input value $r \in R$ has only one associated output value

$$\tilde{r} \in \{\tilde{r}^{(1)}, \tilde{r}^{(2)}, \ldots, \tilde{r}^{(p)}\}.$$

The definition range, which in this case covers the set of real numbers, is therefore subdivided into disjunctive intervals, and each interval is assigned an applicable function value $\tilde{r}^{(i)}$. Normally, the number of intervals exactly corresponds to the power of the value set. The limits between the intervals are denoted as thresholds.

[0038] Figure 4 shows an example of a quantization function graphically, in the form of a characteristic.

[0039] The actual estimation of the transmitted data sequence is based on an apparatus which estimates the state sequence of a channel modelled as an automatic system on the basis of theoretical likelihood considerations, and uses this to determine the most probably transmitted symbol sequence â.

[0040] To do this, the data estimator 11 requires so-called metrics increments which are shown, by way of example, in Figure 7 as elements "1" in a metrics table 14 and which are related to the conditional likelihood of a specific analogue/digital converted value and of a channel state, and in consequence are related to the interference likelihood density.

[0041] One aspect of the present invention is based on obtaining the required metric increments "1" on the basis of channel-state-dependent observation of the information supplied from the quantizer 10. To do this, the events are counted as a function of the states, and the overall required statistical characteristics of the channel can be derived from this. The metrics increments are stored in a table 14, and the number of events is stored in a store 15, which is likewise shown by way of example in Figure 7. Table 14 for the metrics increments "1" is connected directly downstream from the A/D transducer 10, as can also be seen in Figure 5.

[0042] The channel model used in US Patent 5,131,011 generates the possible channel output signals, as a function of the state, in the absence of noise, and the channel estimation method also adaptively determines the noise-free potential output signals. However, this method cannot be used for optimum consequence estimation for non-Gaussian, state-dependent noise. For this reason, the branch metrics Table 14 for the channel model of the invention contains the complete stochastic characteristics of the channel from the point of view of the assessment apparatus, which characteristics are determined adaptively.

Theory of an optimum estimator (MLSE) for quantized signals

[0043] The following text describes the theoretical principles of optimum estimation taking account of an A/D transducer and this estimation forms the basis for the inventive solution to the problem of an optimum estimator.

[0044] The quantizer or A/D transducer provides a function which assigns elements in a finite set to the continuous, real input values. If r denotes the input value of the quantizer and $\tilde{r}$ the output value, then reference is made to equation 1, in which case this functional definition includes the requirement for uniqueness, that is to say each input value $r \varepsilon R$ has only a single associated output value

$$\tilde{r} \in \{\tilde{r}^{(1)}, \tilde{r}^{(2)}, \ldots, \tilde{r}^{(p)}\}.$$

The definition range (in this case the set of real numbers) is thus subdivided into disjunctive intervals, and each interval is assigned an associated valid function value $\tilde{r}^{(1)}$. Normally, the number of intervals just corresponds to the power P of the value set. The limits between the intervals $[s_{i-1}, s_i]$ with which the values $\tilde{r}^{(i)}$ are associated, are referred to as thresholds.

[0045] If $\tilde{r}$ denotes the vector of the quantized samples, then, on the assumption that successive samples are statistically independent, the expression for the maximum likelihood sequence estimator is:

Equation 2

$$\tilde{a} = \arg\{\max_b(p(\tilde{r}|b))\}$$
$$= \arg\left\{\max_b\left(\prod_\mu p(\tilde{r}_\mu|b)\right)\right\}$$

[0046] Since the random variables $\tilde{r}_\mu$ can assume only a finite number of discrete values, the conditional likelihood density function consists of weighted delta pulses. The a priori likelihood $P(\tilde{r}_\mu|b)$ of the occurrence of a specific output value from the quanitizer is therefore used instead of the density function. If it is also assumed that the value r_μ sampled at the discrete time depends only on the L previously transmitted symbols (finite memory), then:

Equation 3

$$\tilde{a} = \arg\left\{\max_b\left(\prod_\mu P(\tilde{r}_\mu|(b_\mu, b_{\mu-1}, \ldots, b_{\mu-L}))\right)\right\}$$
$$= \arg\left\{\max_b\left(\sum_\mu \log P(\tilde{r}_\mu|z_\mu)\right)\right\}$$
$$= \arg\left\{\max_b\left(\sum_\mu l(\tilde{r}_\mu, z_\mu)\right)\right\}$$

[0047] Since both the variable $\tilde{r}_\mu$ and Z_μ can assume only a finite number of different values, the individual branch metrics or elements of the metrics Table 14 can store $1(\tilde{r}_\mu, Z_\mu)$ in a table, which is highly conducive to the hardware implementation, since this Table 14 can be in the form of a store.

[0048] A priori likelihood $P(\tilde{r}_\mu|Z_\mu)$ can easily be determined exactly from the a priori density function $p(\tilde{r}_\mu|Z_\mu)$ of the signal with continuous values. In this case:

Equation 4

$$P(\tilde{r}_\mu|z_\mu) = P(\tilde{r}^{(i)}|z^{(k)})\Big|_{\tilde{r}_\mu = \tilde{r}^{(i)}, z_\mu = z^{(k)}} = P(s_{i-1} < r \le s_i|z^{(k)})$$
$$= \int_{s_{i-1}}^{s_i} p(r|z^{(k)})dr$$

[0049] This means that the a priori likelihood for a specific event corresponds exactly to the area of the a priori likelihood density function between the two associated thresholds, as is shown in Figure 7, which explains the relationship between the likelihood density function and the likelihood distribution of the quantized signal.

[0050] In consequence, the variables $P(\tilde{r}_\mu|Z_\mu)$ required for the optimum estimator can, in a practical implementation, be obtained by measuring the relative frequency, which corresponds to the number of events related to the total number of measurements, with which the samples r_μ lie in an interval $S_{i-1}<r_\mu<S_i$ for a specific channel state $Z^{(k)}$. However, the interval in which a sample lies is precisely the magnitude which a quantizer provides at its output. The digital quantizer output can therefore be used as the address of a memory cell, which is incremented by one for the relevant sample and the relevant state, and thus contains the number of events. After completion of a measurement cycle, the frequency

distribution for each state $Z^{(k)}$ can be deduced from the total number of samples and the memory contents. Since likelihoods in logarithmic form are generally used for calculation purposes, the required branch metrics are obtained by taking logarithms of the frequency values.

[0051] The metrics Table 14, which may also be referred to as a branch metrics table, thus contains those metric increments which can be used directly for a Viterbi algorithm (VA) in the data estimation apparatus 11. The application of the Viterbi algorithm to the values in the metrics Table 14 is well known to persons skilled in the art, and does not require any further explanation at this point.

[0052] Theoretically, it is also possible to verify that these metrics increments or elements in the metrics table are expediently the logarithms of the conditional likelihoods of the respective transitions $1(\tilde{r}_\mu | z_\mu) = -\log P(\tilde{r}_\mu | z_\mu)$. This Table 14 may be implemented by one or more random access memories, in which case the quantized signal then represents the respective address.

Channel estimator

[0053] The channel estimator 13 has the task of estimating the required conditional likelihoods. The channel estimator comprises a delay element for the quantized signal $\tilde{r}_\mu$, a shift register for determining the channel state, and a table for counting the events, and the latter is represented as Table 15 in Figure 6. This Table 15 may be implemented by one or more random access memories, in which case the quantized and delayed signal and the associated estimated state represent the address. The respectively addressed memory cell is incremented by one per symbol clock cycle, so that event counting takes place and a histogram is thus formed for each state.

[0054] If N denotes the number of events per state $\hat{z}^{(i)}$ and it is assumed that $H(\hat{z}^{(i)}, \tilde{r}^{(j)})=H(i,j)$ is the content of the memory cell of state $\hat{z}^{(i)}$ and quantized value $\tilde{r}^{(j)}$, then:

Equation 5

$$P(\tilde{r}_\mu | z_\mu) = \lim(1/N \cdot H(i,j)), \text{ as N tends to infinity.}$$

[0055] This means that, provided N is sufficiently large, the event counting carried out results virtually directly in the conditional likelihood, which is found once again in the expression in the branch metrics for the optimum sequence estimator.

[0056] In order to prevent memory overflows, the memory may be normalized at regular intervals (algorithm, page 5).

Branch metrics calculation (BMC)

[0057] The branch metrics are calculated in the block BMC from the histogram H(i,j). To do this, logarithms are taken of the individual memory contents H(i,j) in the event store 15:

Equation 6

$$BM(i,j) = -\ln(H(i,j))$$

[0058] The elements of the metrics Table 14 obtained in this way are then, as is shown by way of example in Figure 5, transferred by the discrete channel estimator 13 to the metrics Table 14.

[0059] However, it should be remembered that the number of events per state $\hat{z}^{(i)}$ and quantized value $\tilde{r}^{(j)}$ may be very small or zero. For this reason, adaptation algorithms which are known to persons skilled in the art are used to prevent poles from occurring while taking logarithms.

[0060] It is furthermore within the scope of the invention to transmit pilot data or test data first of all before signal transmission starts, which data are distributed statistically or randomly over the various channel states by means of a scrambler or other suitable devices, and to offer the capability to set the estimation apparatus optimally during a test period for it. Such pilot data or test data can, furthermore, be transmitted regularly or as a function of any interference that occurs.

Claims

1. Estimation apparatus in particular having a channel estimator (13) for estimating characteristics of a transmission

channel, in which case the transmission channel is subject to interference, and in which the analogue data (5) received from the transmission channel is assigned an estimator sequence (â) of digital data values in particular by means of a data estimator (11),
which is **characterized**
in that the estimator apparatus produces at least one estimation sequence (â) whose estimation includes both characteristics of the transmission channel and characteristics of the receiver.

2. Estimation apparatus according to Claim 1, in which the analogue input signal (5) is preferably filtered and is analogue/digital converted as a preferably filtered signal r, and the analogue/digital converted value $\tilde{r}$ is assigned a value ($l_{i,j}$) from a metrics table (14).

3. Estimation apparatus according to Claim 2, in which the values in an event table (15) each comprise the number of occurrences of a specific analogue/digital converted value $\tilde{r}_\nu$ in a state (z_μ) of the transmission channel.

4. Estimation apparatus according to Claim 3, in which the state per analogue converted value is obtained from the estimation sequence â of the data estimation apparatus (11).

5. Estimation apparatus according to Claim 4, in which the conditional likelihood $P(\tilde{r}_\nu|z_\mu)$ of the occurrence of the analogue/digital converted value $\tilde{r}_\nu$ for a state z_μ of the transmission channel is obtained from the event table (15).

6. Estimation apparatus according to Claim 5, in which one element in the metrics table (14) corresponds to the logarithm of the conditional likelihood $P(\tilde{r}_\nu|z_\mu)$ of the occurrence of a specific analogue/digital converted value $\tilde{r}_\nu$ in state z_μ of the transmission channel.

7. Estimation apparatus according to one of Claims 2 to 5, in which the conditional likelihood $P(\tilde{r}_\nu|z_\mu)$ of occurrence of a specific analogue/digital converted value $\tilde{r}_\nu$ in a state of the transmission channel after completion of a measurement interval is normalized by forming the ratio with the total number of events N which have occurred for this state.

8. Estimation apparatus according to one of Claims 2 to 7, in which the elements of the metrics table (14) are updated on the basis of the estimation sequences (â) obtained and the analogue/digital converted values.

9. Estimation apparatus according to one of Claims 2 to 8, in which the data estimator (11) is supplied with the associated value set $l_{i,j}$ from the metrics table (14), and which in each case assigns a most likely value of an estimation sequence (â) to the supplied value set $l_{i,j}$ and supplies an output signal to the discrete channel estimator (13), from which the channel estimator (13) determines the state of the transmission channel z_μ.

10. Estimation apparatus according to Claim 9, in which histogram values are obtained from the elements of the event table (15) and are used to carry out continuous calculation of the values of the metrics table (14).

11. Estimation apparatus according to one of the preceding claims 2 to 10, in which the values in the metrics table (14) are each associated with more than one digital/analogue converted value.

12. Receiver for receiving data transmitted by means of a transmission channel, **characterized by** an estimation apparatus according to one of the preceding claims.

13. Receiver according to Claim 12, further **characterized by** a filter 12 and a sampler 8.

14. System for transmitting data **characterized by** a receiver according to Claim 12 and an estimation apparatus according to one of the preceding claims 1 to 11.

FIG. 1

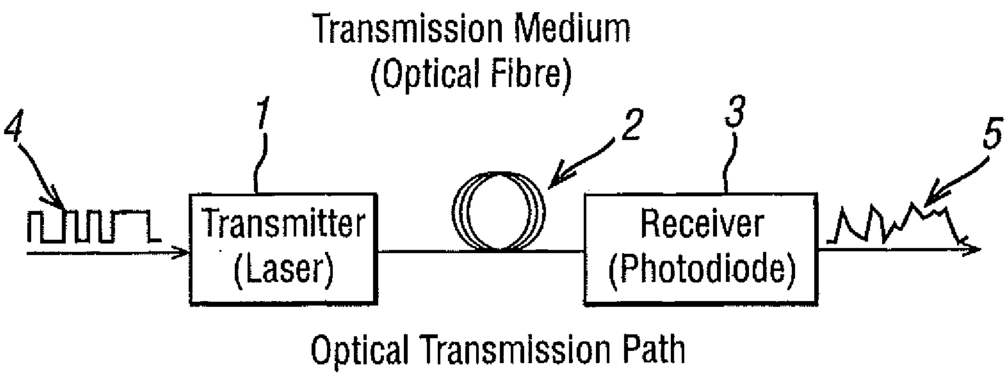
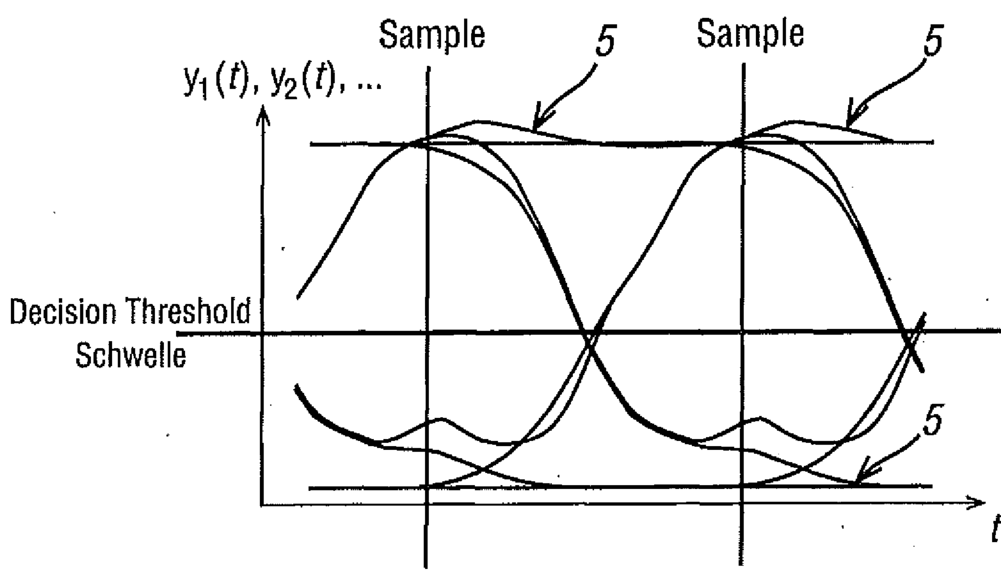


FIG. 2



Eye Diagram Of The Signal Received Without Interference On An Optical Transmission Path

FIG. 3a

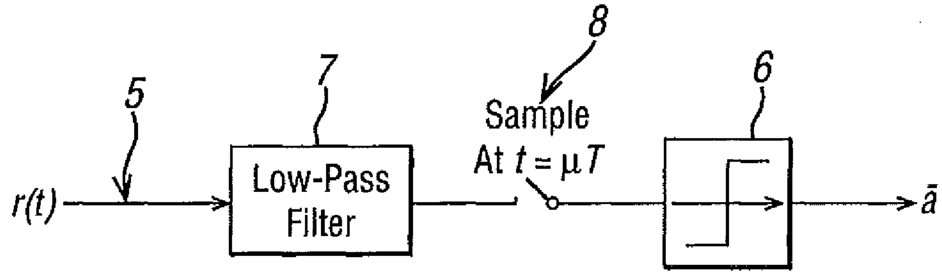


FIG. 3b

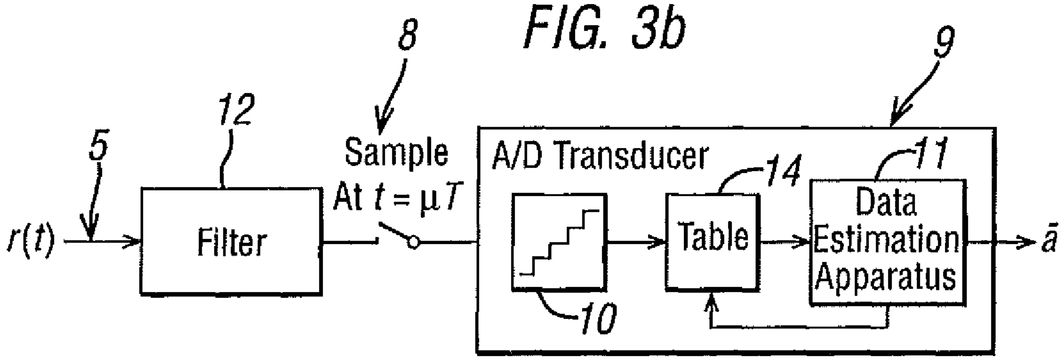


FIG. 4

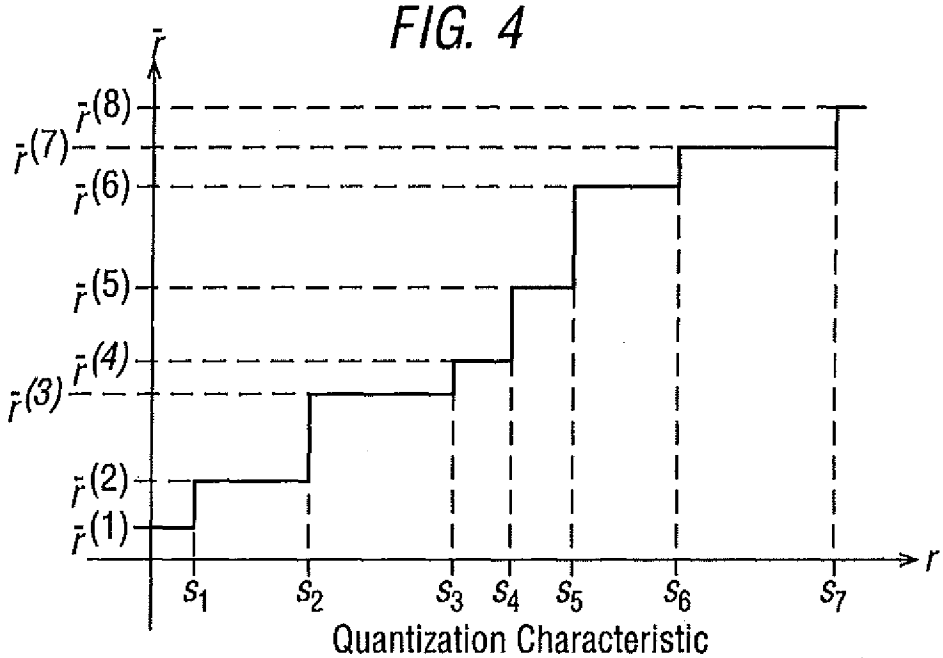
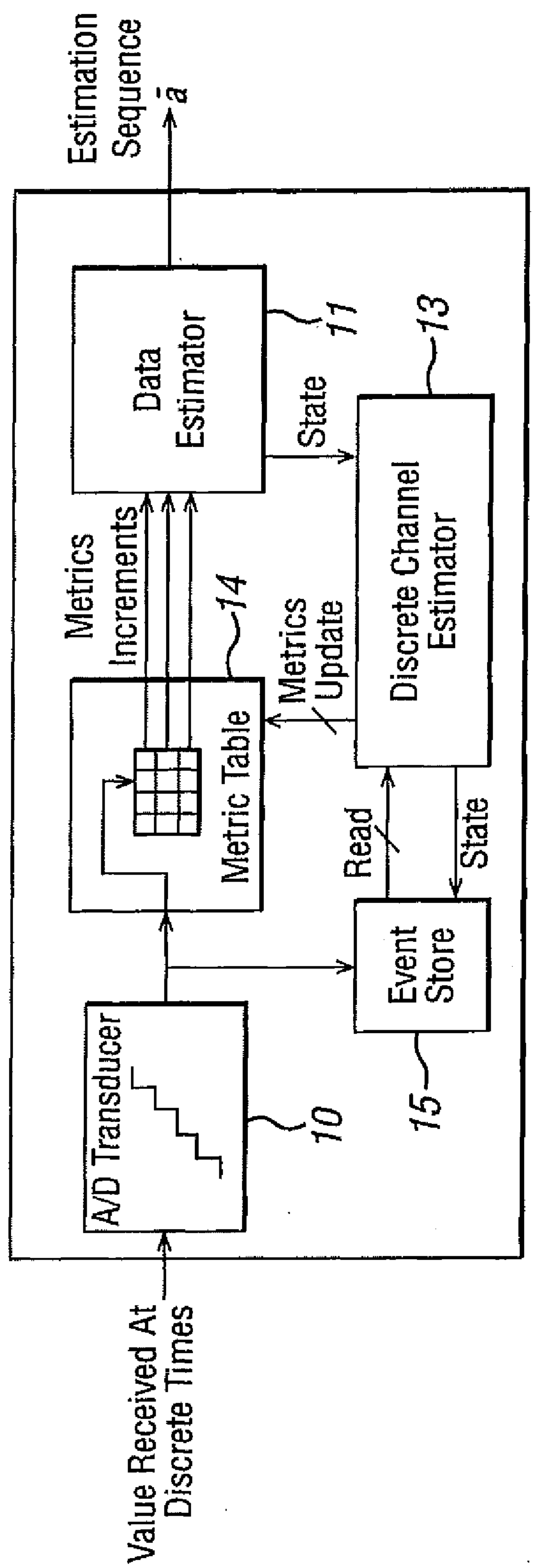


FIG. 5



Block Diagram Of The Invention

FIG. 6

Event Store

15

Quantized Value

	$\bar{r}(1)$	$\bar{r}(2)$	$\bar{r}(3)$	------	$\bar{r}(2^b)$
$z(1)$	n_{11}	n_{12}	n_{13}		n_{12^b}
$z(2)$	n_{21}	n_{22}	n_{23}		
State $\vdots$					
$z(q^k)$	n_{q^k1}				$n_{q^k2^b}$

e.g Functional Map Or Algorithm

Metrics Table

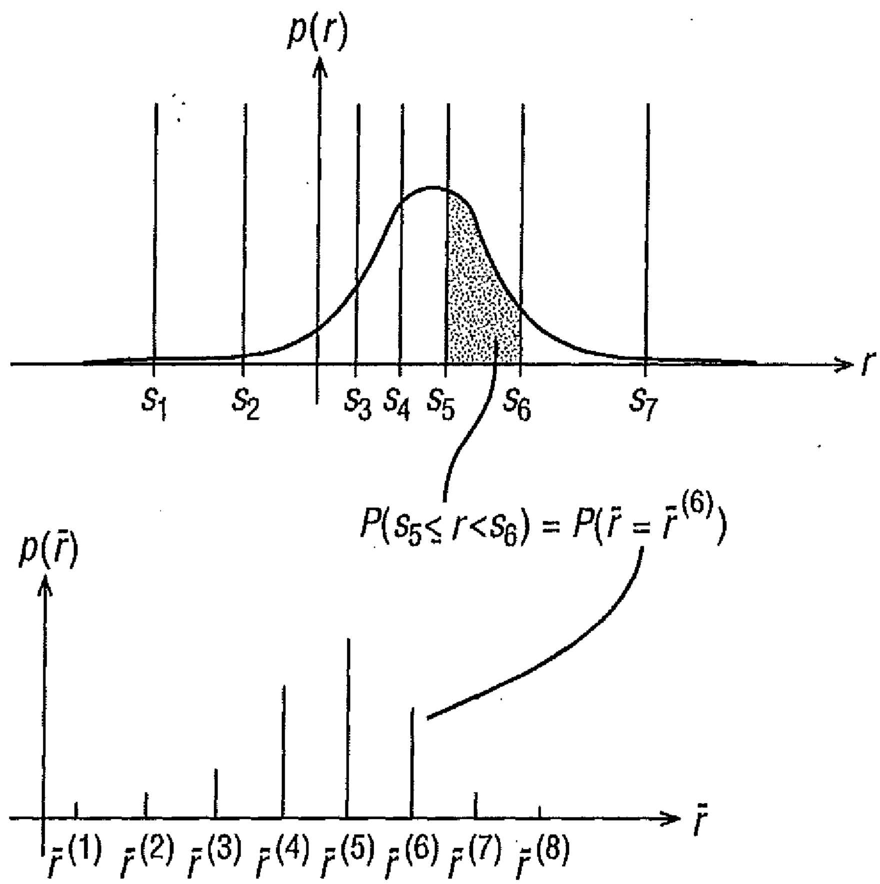
14

Quantized Value

	$\bar{r}(1)$	$\bar{r}(2)$	$\bar{r}(3)$	------	$\bar{r}(2^b)$
$z(1)$	l_{11}	l_{12}	l_{13}		l_{12^b}
$z(2)$	l_{21}	l_{22}	l_{23}		
State $\vdots$					
$z(q^k)$	l_{q^k1}				$l_{q^k2^b}$

Event Table And Table Of The Metrics Increments

FIG. 7



Relationship Between The Likelihood Density Function
And The Likelihood Distribution Of The Quantized Signal

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 31 1162

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 887 027 A (COHEN HERBERT B ET AL) 23 March 1999 (1999-03-23) * abstract * * column 1, line 26 - line 29 * * column 2, line 24 - line 37 * ---	1,12-14	H04L25/02
A	US 5 432 821 A (RAHELI RICCARDO ET AL) 11 July 1995 (1995-07-11) * abstract; figure 14 * * column 5, line 14 - line 18 * * column 11, line 38 - line 41 * * column 12, line 42 - line 52 * * column 13, line 30 - line 60 * ---	1-5,8-10	
A	HIROSHI KUBO ET AL: "AN ADAPTIVE MAXIMUM-LIKELIHOOD SEQUENCE ESTIMATOR FOR FAST TIME-VARYING INTERSYMBOL INTERFERENCE CHANNELS" IEEE TRANSACTIONS ON COMMUNICATIONS,US,IEEE INC. NEW YORK, vol. 42, no. 2/03/04, 1 February 1994 (1994-02-01), pages 1872-1880, XP000447401 ISSN: 0090-6778 * figure 4 * * page 1875, left-hand column, line 24 - line 36 * * page 1876, left-hand column, line 24 - line 30 * -----	1-5,8-10	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	2 July 2001	Papantoniou, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 31 1162

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
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02-07-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5887027 A	23-03-1999	EP 0930750 A	21-07-1999
		JP 11266186 A	28-09-1999
		TW 406486 B	21-09-2000
US 5432821 A	11-07-1995	NONE	

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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(71) Applicant: CoreOptics GmbH
90411 Nürnberg (DE)

(72) Inventors:
- Langenbach, Stefan
90411 Nürnberg (DE)
- Nebojsa, Stojanovic, Prof. Dr.
90411 Nürnberg (DE)
- Ulrich, Boecker
90411 Nürnberg (DE)

(74) Representative: Hellmich, Wolfgang, Dr.
c/o Grünecker, Kinkeldey, Stockmair & Schwanhäusser,
Maximilianstrasse 58
80538 München (DE)

(54) **Error rate estimation method for a receiver and receiver apparatus**

(57) This invention relates to a method for a receiver. The method comprises receiving a sequence of symbols. Further an unreliable detection event is determined, if the absolute value of a difference between a first metric for a first event minus a second metric for a second event is lower than a predetermined threshold. Moreover a receiver is provided, the receiver comprising a metric generator for generating a first and a second metric, and an unreliability detector for detecting an unreliable detection event.

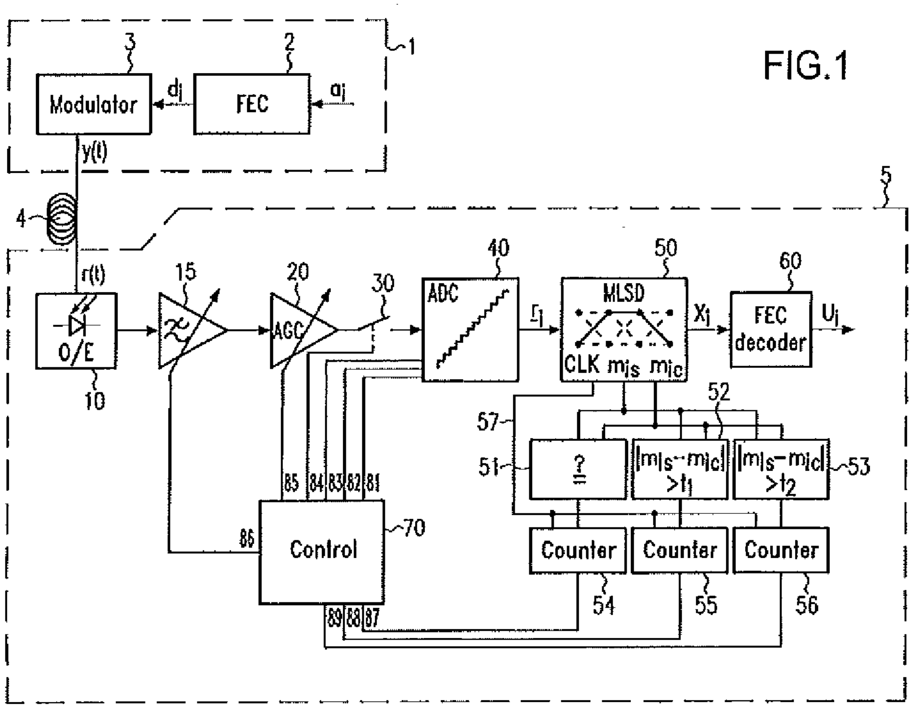

FIG.1

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Description

[0001] The present invention relates to a method and a receiver according to the preamble parts of claims 1 and 15, respectively. In particular the invention relates to the detection of an unreliable detection event (UDE) providing a basis for error rate estimation.

[0002] In digital receivers it is often necessary to continuously estimate receiver performance in terms of the "quality" of the detected digital output signal. The on-line estimation of receiver performance may be used to improve transmission quality, for instance by initiating the use of redundant transmission resources providing better transmission quality (e.g. channel switching in wireless applications).

[0003] Error rate and, more specifically, Bit Error Rate (BER), is universally accepted as a service oriented "quality" measure of performance of a digital transmission system. Sometimes, an errored-block rate (EBR) is used instead of BER, because the EBR is easier to measure. However, for practical purposes and for not-too-long block lengths, the difference between BER and EBR often becomes irrelevant, especially at high signal-to noise ratios (SNR), i.e. at very low BER, when most errors occur in isolation.

[0004] Determination of true error rate is clearly impossible without knowing the transmitted bit stream, so one must resort to error rate estimation.

[0005] Unfortunately, in order to minimize error rate, measurements of physical signal parameters that are directly related to the controllable receiver parameters, like received signal strength, power, etc., are often insufficient for control, because the dependence of the error rate on these parameters is unknown, especially for heavily distorted signals which are processed by non-linear processing functions, as is the case e.g. in a maximum-likelihood sequence detector (MLSD).

[0006] Measuring physical signal parameters, such as received signal strength provides only a very crude measure of overall system performance in particular the error rate. Hence such measured signal parameters are hardly suitable to optimize receiver parameters for minimum error rate. Only in some simple applications, such "local" performance optimization is possible, e.g. when adapting sampling phase towards maximized eye opening in a transmission system with hard-decision detection and with a channel without significant inter-symbol-interference (ISI). But typically such optimizations do not work under harder conditions, e.g. when severe ISI occurs or when a more complex detector is used.

[0007] In a digital communication system symbols are transmitted and typically a number of 2^n symbols are used. In the binary case (n=1), there are two different symbols, designated logic 0 (zero) and logic 1 (one).

[0008] In a well-known approach, bit error rate (BER) estimation is accomplished with the help of a Forward Error Correction (FEC) decoder, e.g. by counting the number of corrected bit positions. However, this **FEC based estimation** does not work well when FEC decoder errors are dominant i.e. at very low SNR. Another drawback is that the method requires a long feedback path from a downstream FEC decoder, which may be designated receiver back-end, to the receiver front-end, typically comprising demodulator and detector. Yet in some applications no FEC decoder may be present, or a framing-agnostic and FEC-agnostic method of estimation may be used instead. The latter may be the case when the FEC decoder is administratively separated from the front-end i. e. when the front end is a stand-alone product, and hence the receiver back-end may not provide the necessary BER estimation feedback. E.g. the FEC decoder may be located in a host system's digital receiver back-end of a separately marketable dense wave division multiplexer (DWDM) transponder module that comprises a optical-to-electrical (O/E) and an analog-to-digital (A/D) conversion and a symbol detector, but no FEC decoder.

[0009] In another conventional embodiment, the detected or decoded bit stream is compared with a known periodically repeated transmission sequence, i.e. a **training-based estimation** is carried out. This method has the disadvantage of training sequence overhead, which causes a rate increase, which in turn is extremely undesired in case of bandwidth-limited optical transmission systems, such as DWDM systems. Moreover the method requires knowledge of data formats.

[0010] Both FEC based methods and training-sequence-based methods require a framing process and do not work on un-synchronized bit streams.

[0011] In a **metrics-based estimation** approach, decision information in a Viterbi decoder or detector, which will be explained below, is used for providing a basis of a BER estimation.

[0012] US 5,944,844, "Method for determining connection quality in a receiver utilizing a Viterbi Decoder". This invention uses accumulated path metric differences, i. e. the sum of decision variables and the minimum of decision variables along the decoded path in the VA (Viterbi algorithm) to estimate BER. A drawback of this method is an increase of complexity since decision variables need to be stored until the trace-back step is completed and since accumulation of decision variable introduces complexity due to a floating-point format. Apart from the disclosure to compare estimates with predetermined threshold values the US 5,944,844 fails to expose a practical mapping from the measured observable to a BER estimate.

[0013] US 6,141,388, "Received signal quality determination method and systems for convolutionally encoded com-

munications channels". Unlike the method of US 5,944,844, rather than using decision variables accumulated along the decoded path, this invention uses only the final decision metric in a decoded frame. This final decision metric is then mapped to a BER estimate. The method is described only in connection with convolutionally encoded data streams and frame decoding. Again, there is no disclosure how to map the measured decision metrics to a BER estimate.

[0014] A. J. Viterbi proposed in "Error Bounds for Convolutional Codes and an Asymptotically Optimum Decoding Algorithm" (IEEE Trans. Inf. Theory, IT-13, pages 260 to 269, April 1967) a decoding algorithm for convolutional codes, which has since become known as the **Viterbi algorithm.** Later on it was recognized that it was in fact a maximum-likelihood decoding algorithm for convolutional codes (confer Shu Lin, Daniel J. Costello Jr., "Error Control Coding: Fundamentals and Applications" Prentice-Hall, Inc., Englewood Cliffs, New Jersey 07632, 1983).

[0015] The Viterbi algorithm may also be used for channel equalization in order to cope with ISI. On a binary ISI channel, at a channel memory of m bits, there are 2^m states corresponding to all possible bit sequences of length m and 2 transitions entering and leaving each state, i.e. there are 2^{m+1} transitions between successive stages or time units in the trellis.

[0016] In an initializing step of the Viterbi algorithm beginning at an initial stage a path metric for a single path entering each state at the initial stage is computed. Each transition between states corresponds to a symbol. The path and its path metric is stored for each state.

[0017] The Viterbi algorithm further comprises a repeating step. In the repeating step the path metric for all the paths entering a state at a stage is computed by adding the branch metric entering that state to the metric of the connecting survivor at the state of the preceding stage. For each state the path with the largest path metric, called survivor path, is stored together with its path metric, and all other paths are eliminated.

[0018] A log-likelihood function log P(r|v) is called the metric associated with the path v and is denoted M(r|v). The different metrics depend on the properties of the transmission path. They may be obtained from noise measurements. The metrics may be assumed to be time invariant and listed in a look-up table for each transition from one state to another for a special application, or it may be obtained from on-line measurements (cf. EP 1 139 619 A1 "Channel estimation using a probability mapping table").

[0019] In a **truncation mode Viterbi detector,** path memories are truncated after D symbols and a decision is enforced on transitions to the states that are leaving the "window" of D+1 trellis stages. More specifically, such a detector has a path memory that contains D+1 trellis stages resulting in D transitions. When computing survivors from time t+1, a decision on the detector output is forced for a specific transition from a state at time instant t-D to a state at time instant t-D+1. As usual, in a practical implementation the states on this selected transition could be the trace-back states on the best path at time t, or they could be traced back from any state at time t.

[0020] A Viterbi detector operating in block-mode **(block-mode VA)** detects bits in a block i.e. a trellis segment by finding the best path between two previously determined states at the block boundaries. For the purpose of this invention, it is immaterial which detailed method is used to determine the states at the block boundaries.

[0021] For highest throughput applications like high-speed optical communication systems operating at data rates e. g. at 10 Gbps or 40 Gbps or above, it is essential that the error rate estimator can be implemented with very low additional complexity.

[0022] It is the object of this invention to provide a method and a receiver using another observable which does not require extensive calculations and/or additional circuitry.

[0023] This object is achieved by the subject matter of the independent claims.

[0024] Preferred embodiments of the invention are the subject matter of the dependent claims.

[0025] This invention advantageously does not require a framing process and can operate on non-synchronized bit streams, unlike both the FEC-based methods and the training-sequence-based methods. So the present invention does not require a FEC code nor a known training sequence for error rate estimation.

[0026] Advantageously the same principle can be applied for symbol detectors, maximum-likelihood-sequence detectors, truncation mode sequence detectors, block processing sequence detectors, and frame decoders for trellis encoded frames. This means that this invention can be applied to all detectors and decoders where a random decision can be identified.

[0027] In the binary case i.e. if only two symbols designated logic 0 and logic 1 are sent and detected on the receiver side the unreliable detection event can be determined by checking as to whether the analog voltage is within a range around the threshold which is used for discriminating logic 0 and logic 1. The latter step is a kind of an analog-to-digital conversion.

[0028] As a further advantage, the additional condition may be used that a decision must be a relevant random decision, i.e. a random decision where a wrong decision necessarily leads to a bit error. This additional condition ensures that only events are considered which are related to the bit error rate, by definition.

[0029] The advantage of considering more than one unreliable detection events by different thresholds for the absolute value of the metric difference between survivor and competitor generates more observables for the error rate e.g. the unreliable detection events obtained by using a lower threshold may be allowed for in the case of lower bit

error rates and vice versa.

[0030] The condition that two metrics are equal in case that the metrics are represented by digital values can be verified by a single operation in most processors after the metrics have been loaded into appropriate registers. This illustrates that dedicated logic for checking the equality of two registers requires only a small amount of dedicated circuitry.

[0031] Counting unreliable detection events during a fixed period of time and reading the counter value thereafter results in a value which is proportional to the frequency of the unreliable detection events, which in turn is related to a bit error rate approximately by simple equation (8).

[0032] The adaptation of the period of time for counting the unreliable detection events to the frequency of the unreliable detection events may ensure quick adaptation of the receiver parameters in order to minimize the bit error rate and to ensure a sufficiently small uncertainty in the frequency of detection events.

[0033] If the counter value is considered to be too small i. e. lower than a first threshold, the counter value is preferrably not reset, such that the current measurement period is extended and accumulated values are not discarded..

[0034] The setting of demodulator parameters in order to minimize the unreliable detection event frequency and thereby the bit error rate keeps the bit error rate at an optimum even if the channel properties change in time.

[0035] In the following preferred embodiments of this invention are described referring to the accompanying drawings. In the drawings:

Fig. 1 shows an optical transmission system,

Fig. 2 illustrates the unreliable detection event for binary symbols; and

Fig. 3 and Fig. 4 show simulation results.

Abbreviations:	
A/D: analog-to-digital	ADC: analog-to-digital converter
AGC: automatic gain control AWGN: additive white Gaussian noise BER: bit error rate DWDM: dense wave division multiplexer EBR: errored-block rate FEC: forward error correction ISI: inter-symbol interference	MLSD: maximum-likelihood sequence detection O/E: optical-to-electrical PDF: probability density function PMD: polarization mode dispersion RDE: reliable detection event SNR: signal-to-noise ratio UDE: unreliable detection event VA: Viterbi algorithm

[0036] An embodiment comprises a low-complexity error rate estimation method based on information that is readily available in a Maximum-Likelihood-Sequence-Detector (MLSD). It is especially useful for a local error-rate-based control loop within a digital receiver front-end (demodulator and detector).

[0037] More specifically, detection performance of a MLSD receiver, in terms of minimizing post-detection error rate is optimized, by providing a low-complexity post-detection error rate estimate to a receiver control facility for unframed data streams.

[0038] To this end "unreliable detection events" (UDE) are detected, counted, optionally processed, and then used to estimate error rate.

[0039] Fig. 1 shows an optical transmission system. It comprises a transmitter 1, and optical link 4 and a receiver 5. A typical transmitter 1 comprises an FEC encoder 2 for encoding input data a_i in order to generate data d_i. This data d_i is forwarded to a modulator 3. The modulator 3 generates an optical signal y(t) constituting the output of transmitter 1.

[0040] The optical signal is transmitted via optical link to receiver 5. The optical link comprises optical fibers which attenuate the optical signal and in addition constitute a dispersive channel. In order to compensate for the attenuation the optical link may comprise optical amplifiers which add noise to the optical signal. In state of the art dense wave division multiplexer (DWDM) systems the optical signal suffers from severe signal distortions that are caused by chromatic dispersion or group velocity dispersion, polarization mode dispersion (PMD), self-phase-modulation, inter-symbol interference (ISI) caused by the receiver itself, and other signal distortions that can beneficially be removed or counteracted by means of a MLSD.

[0041] At the receiver side of the optical link the optical signal r(t) is input into receiver 5. Receiver 5 comprises

physical interface 10 which performs an O/E conversion. The analog electrical signal may be directly input into automatic gain control (AGC) circuit 20. Both, the physical interface 10 and AGC circuit 20 comprise an upper cut-off frequency. Both cut-off frequencies must be higher than 1/(2T), T being the symbol period. On the other hand too much excess bandwidth in excess over the required minimum picks up more noise from the optical link 4, which degrades the receiver performance by increasing the bit error rate. In typical receiver designs an excess bandwidth of 50% to 100% is therefore provided (S. U. H. Qureshi, "Adaptive equalization", Proc. IEEE, Vol. 73, 1985, pp. 1349-1387).

[0042] In practice due to the design complexity of low pass filtering in the GHz range, often only implicit low pass filtering is performed in the receiver, by virtue of given component bandwidth limitations. However, in order to obtain a more precise control of the bandwidth, another embodiment may comprise an adjustable low pass filter 15 between physical interface 10 and AGC circuit 20. The low pass filter 15, especially its cut-off frequency, is controlled by output 86 of control unit 70 in order to minimize the bit error rate.

[0043] The AGC circuit 20 may amplify the analog electrical signal output either by physical interface 10 or low pass filter 15 to a constant level in terms of average rectified voltage or root-mean-square voltage. In another embodiment the amplification of AGC circuit 20 may be controlled by control unit 70, output 85 based on digitized values r_j (cf. US 3,931,584).

[0044] The sampling phase of A/D converter (ADC) 40 may be controlled by a sample-and-hold circuit 30 illustrated by a switch in Fig. 1. The sample-and-hold circuit 30 is controlled by output 84 of control unit 70. The ADC 40 performs a three-bit conversion and outputs digital data r_j. Various parameters of the ADC 40 may be controlled by control unit 70. Therefor outputs 81 to 83 of control unit 70 are provided. Output 81 may control the offset of ADC 40, output 82 may provide a reference voltage which controls the amplification of the A/D conversion i. e. the spacing of the thresholds and output 83 may control the non-linearity of the ADC 40.

[0045] In other embodiments an N-bit conversion may be performed by the ADC 40, wherein N is an integral positive number.

[0046] The digitization of the analog signal output by AGC circuit 20 may be performed at the symbol rate of 1/T. In another embodiment n-fold over-sampling may be performed i.e. the analog voltage output by AGC circuit 20 is sampled at a rate of 1/(nT). The sampling rate is controlled by control unit 70, which controls the sample and hold circuit 30 and the digitization of ADC 40. In high-speed applications n is often chosen to be 2 since higher values of n are not feasible due to component restrictions. In the case of n=2 the rising and falling clock edges can be used to trigger sampling based on a recovered symbol clock. The symbol r_j output by ADC 40 is input into MLSD 50 which may be implemented by a Viterbi decoder. More specifically the Viterbi decoder may be of a truncation mode type or a block mode type. As explained above a Viterbi decoder determines the most likely path, designated survivor, on the basis of metrics. The metric of the most likely path is output at output m_{ls} of MLSD 50. The metric of the best competitor path is output at output m_{lc} of MLSD 50.

[0047] In the case of a Truncation Mode Viterbi Detector a UDE is declared if the survivor decision at time t-D was a random decision. The only addition to the standard Viterbi detector is an additional memory containing the information about path metric equality, one bit per stage and state. This memory is required due to the delay of D steps between detecting path memory equality and using that decision.

[0048] In another embodiment a UDE can also be defined and detected if a VA is run to determine a most likely state at a particular stage of the trellis, starting from identical zero path metrics. A UDE may only be declared if this best state selection is subsequently used for detection, i.e. when it is relevant.

[0049] In some trellises estimation of bit error rate can be improved if a UDE is declared not for arbitrary path metric equalities, but only for path metric equalities between the best path that detects a one on a specific transition and the best path that detects a zero on that specific transition.

[0050] MLSD 50 outputs the detected symbols of the most likely path X_l to FEC decoder 60. The FEC decoder 60 finally outputs data U_j. In one embodiment the FEC decoder 60 is designed to work with a relatively high input BER of e.g. 10^{-4} and still provide a very low output BER of e.g. 10^{-15}. This situation is common in modern optical high-speed systems such as DWDM systems employing so-called advanced FEC.

[0051] Unreliable detection events may be declared if the metrics of the survivor and competitor path are equal which is detected in comparator 51. A second kind of UDE may be declared if the absolute value of the difference between the metrics of the survivor and competitor paths are lower than a threshold t. This condition is checked in comparators 52 and 53 for two thresholds t_1 and t_2. There are embodiments of this invention that comprise only comparator 51 or comparator 52. Other embodiments comprise both comparators 51 and 52. In further embodiments more than two comparators 52 and 53 may be provided with or without comparator 51, wherein each of the comparators 52 and 53 checks for a different threshold t.

[0052] MLSD 50 provides a decision clock on line 57 to counters 54, 55 and 56. The decision clock comprises a pulse each time a decision is to be evaluated. In the case of truncation mode Viterbi detection, the MLSD generates a decision clock pulse each time a decision is enforced after D+1 trellis stages. In the case of block mode Viterbi detection, a decision clock pulse is generated each time a block of data is detected. Each of the counters is enabled

by the decision clock on line 57 and is incremented if the respective comparator has detected an UDE. The counters are read from time to time by control unit 70 via lines 87 to 89 and reset if decided by control 70. The counter values are proportional to the frequencies of unreliable detection events that are evaluated in control unit 70. The control unit 70 may read and reset the counters after a fixed counting period. This period may be different for each counter.

[0053] In another embodiment the counting period of each counter may be adapted to the frequency of UDE. To this end two thresholds may be provided for each counter.

[0054] If the counter value is lower than the first threshold, the counting period is considered to be too short. Consequently the counting period is increased and the counter may be reset. Alternatively the counter value is not reset and counting is continued for the difference between the old and the new counting period before the counter value is read out again and compared to the two thresholds. In high frequency applications, the operations of reading out the counter value, comparing it to two thresholds, calculating a new counting period and the difference between new and old counting periods can not be completed within one detection clock cycle. Consequently one ore more UDEs may be detected and counted meanwhile. In order to avoid incorrect measurements the counter may be disabled until the new counting period is determined.

[0055] If the read out counter value is greater or equal to the first threshold and smaller or equal to the second threshold, the counter value is considered to be in the right range and the counting period remains unchanged. After reading and processing the counter value the respective counter is reset.

[0056] It the counter value is greater than the second threshold the counter value is considered to be too great and consequently the counting period is decreased. After reading and processing the counter value the respective counter is reset.

[0057] In order to avoid too many changes of the counting periods and the computational effort associated herewith, the counting periods may be kept constant for a predetermined number of counting periods. The latter additional rule may only be applied after the first time after power up or reset the counting period is within the first and second thresholds i. e. has reached the target range.

[0058] The control unit 70 may average or smooth read out counter values or the frequencies of UDEs obtained therefrom. The control unit can obtain BER estimates from the UDE frequencies or counter values by equation (8), which will be explained below.

[0059] The control unit 70 may perform a gradient search over the estimated error rate in order to set one or more receiver parameters in order to arrive at an error rate as low as possible. More specifically, in the absence of "locally" measurable "physical" quality indicators, steepest-descent minimization of estimated error rate can be used to optimize such parameter settings, at least when the error rate has a convex functional dependency on the parameter(s) in question, i.e. where a unique globally minimal error rate exists over the relevant parameter space. Error rate optimization is especially beneficial if channel parameters e.g. properties of optical fiber 4 or physical interface 10, often comprising a photo diode, change gradually. In other embodiments the control unit may perform the gradient search on one or more UDE frequencies or counter values. Moreover the control unit 70 may set the gain of the automatic gain control circuit 20 via output 85. A further receiver parameter is the cut-off frequency of low-pass filter 15 which can be set via output 86 of control unit 70. Further the control unit 70 can control the sampling times by sample-and-hold circuit 30 via line 84. Then the control unit influences the thresholds of the ADC 40 via outputs 81 to 83.

[0060] Skilled persons will understand that not all circuit parts may be present in receivers according to this invention. Controlling the sampling phase in sample and hold circuit 30 is especially beneficial in receivers that do not perform over-sampling.

[0061] If a high order low-pass filter is used for low-pass filter 15 the high order low-pass filter generates additional inter-symbol interference, which can be handled by the MLSD 50. There is a perfomance trade-off between noise reduction and increased ISI, which varies with channel parameters. The control unit 70 can adjust the receiver parameters to gradually changing channel parameters by a gradient search over e.g. estimated error rate as explained above.

[0062] In the following the concept of unreliable detection events will be explained in more detail.

[0063] A relevant decision is a decision made in the detector, which is part of a receiver, such that a wrong decision *necessarily* leads to one or more errors in the detected output symbol stream. For instance, in a Viterbi Detector, selecting the wrong incoming branch as a survivor at some state in the trellis is not a relevant decision if the selected branch eventually is not on the survivor. Since the MLSD 50 outputs a decision clock at line 57 indicating a final decision on the path all decisions taken by comparators 51, 52 and 53 are relevant decisions.

[0064] A decision is called a random decision if it is made without sufficient information which alternative is more likely to be correct than the other(s). A strict random decision is a random decision under total indifference amongst alternative(s), e.g. when a decision is made in a Viterbi detector between two alternative paths with exactly identical metrics. This means that decisions detected by comparator 51 are strict random decisions.

[0065] A wide-sense random decision is a random decision under *approximate* indifference amongst alternative(s), e.g. when a decision is made in a Viterbi detector between two alternative paths with an absolute path metric difference that is smaller than some small, predetermined threshold value. Consequently comparators 52 and 53 detect wide-

sense random decisions.

[0066] In this patent, an Unreliable Detection Event (UDE) can be defined as an event that fulfills one or more of the following conditions:

- The event occurs in a detector that is part of a receiver.
- The detector makes a random decision.
- The random decision is a relevant decision, i.e. it affects the detected output symbol stream.

The events detected in comparators 51, 52 and 53 fulfill all of the three conditions above.

Instead of an exact theoretical derivation of the relationship between the UDE frequency and BER or EBR two simplified cases are considered.

The first scenario is "artificial" and only motivates, why observing the frequency of unreliable detection event can give information about the true error rate, in a idealized setting. The results of this scenario apply to both, Symbol or Sequence Detection.

A hypothetical binary "genie" receiver R with the following properties is considered:

[0067] Receiver R decides either completely reliable i. e. error-free or completely unreliable i. e. at random, for a symbol or for a sequence e. g. a block, and R also knows perfectly when an unreliable detection event has occurred because it provides perfect reliability information.

[0068] It is assumed that

- the probability of the event UDE to detect unreliably is P_{ud}
- The probability of the reliable detection event (RDE) to detect reliably is $1-P_{ud}$

[0069] In this case

- the conditional probability $P(e|RDE)$ of the event e to cause an error, in case of reliable detection, is 0.0 (perfect decision)
- the conditional probability $P(e|UDE)$ of the event e to cause an error, in case of unreliable detection, is 0.5 (random decision)

[0070] The total probability of error $P(e)$ at the output of R is $P(e) = 0.0\ P_{ud} + 0.5\ P_{ud}$ which provides a linear relation between the probability P_{ud} of an unreliable detection event and the error probability being equivalent to the error rate.

[0071] Hence, an observer counting the occurrence of unreliable detections, as declared by R, over a sufficiently period of time, can estimate P_{ud} from the relative frequency of unreliable detection events. By virtue of the relation $BER = 0.5\ P_{ud}$, he can then estimate the error rate.

[0072] The second scenario is for a binary symbol detector on Additive White Gaussian Noise (AWGN). This case is much easier to model mathematically since it is simpler than a MLSD as addressed in this invention.

[0073] The method described there could be generalized as another BER estimation method for symbol detectors. Actually, it is a special case of the general approach to derive an estimate of the error rate from a measurement of the amplitude distribution function. Knowing the amplitude distribution function empirically, model distributions for the conditional distributions for each possible symbol could be fitted, and the BER could then be derived analytically from these distributions. Similar techniques are used in simulation software such as VPItransmissionMaker™, albeit based on full knowledge of the transmitted bit sequence.

[0074] Assume a binary random data stream transmitted using binary amplitude modulation over a memory-less channel with AWGN and a bit detector. The a-priori probabilities of sending a one, P(1), and of sending a zero, P(0), are assumed to be identical. Further noise is assumed to be signal-independent, i.e. identical additive noise distribution and hence identical variance σ^2 for received one and zero. More specifically, let u_1 (104) and u_0 (103) be the amplitudes of a received one or zero, respectively, in the absence of noise (cf. Fig. 2). Under the above assumptions the conditional probability density function (PDF) of observing amplitude u, conditioned on the event of a sent one or zero, is

$$p(u\,|\,1)=\frac{1}{\sqrt{2\pi\sigma^2}}\exp\left(-\frac{(u-u_1)^2}{2\sigma^2}\right) \qquad (1)$$

and

$$p(u\,|\,0)=\frac{1}{\sqrt{2\pi\sigma^2}}\exp\left(-\frac{(u-u_0)^2}{2\sigma^2}\right), \qquad (2)$$

respectively (cf. 108, 107, respectively).

[0075] The optimum decision threshold is at the amplitude where the two conditional PDFs assume equal values, which is at the threshold $\Theta=(u_1+u_0)/2$ (cf. 105). The graphs of $p(u|1)$ and $p(u|0)$ as well as Θ are plotted in Fig. 2.

[0076] With this decision threshold, the observed probability of bit error $P_b(e)$, alias BER, is known as

$$P_b(e)=\frac{1}{2}\cdot\operatorname{erfc}\left(\frac{1}{\sqrt{2}}\cdot\frac{d}{2\sigma}\right) \qquad (3)$$

where d is the distance between u_1 and u_0, $d=|u_1-u_0|$. With the well-known approximation

$$\operatorname{erfc}(x)=\frac{1}{\sqrt{2\pi}x}\exp\left(-x^2\right)$$

(for $x\to\infty$), we can write this as

$$P_b(e)\approx\sqrt{\frac{2}{\pi}}\cdot\frac{\sigma}{d}\cdot\exp\left(-\frac{d^2}{8\sigma^2}\right) \qquad (4)$$

[0077] On the other hand, unreliable detection occurs when we observe a received amplitude u with approximately equal distance from u_1 and u_0 is observed, i.e. when $\Theta=u$. In this case $|u-u_1|=|u-u_0|=d/2$ and equation (5) is obtained from equations (1) and (2).

$$p(u=\Theta\,|\,1)=p(u=\Theta\,|\,0)=\frac{1}{\sqrt{2\pi}}\cdot\frac{1}{\sigma}\cdot\exp\left(-\frac{(d/2)^2}{2\sigma^2}\right) \qquad (5)$$

[0078] In this case, deciding for either one or zero is a strict random decision, i.e. the decision is incorrect with a probability of 0.5.

[0079] The probability mass P_{ud} of an unreliable detection event $P(\Theta - \Delta u/2 \le u \le \Theta + \Delta u/2)$ is then approximately

$$P_{ud} \approx \Delta u \cdot (P(1) \cdot p(u = \Theta \mid 1) + P(0) \cdot p(u = \Theta \mid 0)) = \Delta u \cdot \frac{1}{\sqrt{2\pi\sigma^2}} \cdot \exp\left(-\frac{(d/2)^2}{2\sigma^2}\right) \qquad (6)$$

[0080] Taking logarithms and choosing $\Delta u=\gamma \cdot d$ as a multiple of d, equations (6) and (7) are obtained:

$$\ln(P_{ud}) = \frac{1}{8} \cdot \left(\frac{d}{\sigma}\right)^2 + \ln\left(\frac{d}{\sigma}\right) + \ln(\gamma) - \ln\left(\sqrt{2\pi}\right) \qquad (6)$$

$$\ln(P_b(e)) \approx \ln(P_{ud}) + \ln(2) - \ln(\gamma) - 2\ln\left(\frac{d}{\sigma}\right) \qquad (7)$$

[0081] For large d/σ, the log-probability $\ln(P_{ud})$ is dominated by the term quadratic in d/σ. and $\ln(P_{ud})$ equals $\ln(P_b(e))$ apart from additive constants and apart from the term logarithmic in d/σ which becomes negligible for large d/σ, i. e. for low error rates.

[0082] The relationship between logarithmic bit error probability and logarithmic probability of an unreliable detection event is monotonic up to some high BER value, for $d/\sigma > 1$. Hence it is invertible in this range. In general, P_{ud} can thus be used to predict $P_b(e)$ approximately provided that γ is known, or it can be mapped via a lookup-table.

[0083] For instance, in the context of sampling phase adjustment for a given channel, noise variance σ^2 may be assumed to be constant, but the distance d between mean values of one and zero will vary, and consequently BER will vary as well. When we assume that an AGC circuit is used, d will remain about constant but the noise σ^2 will be amplified such that again the "signal-to-noise ratio" d^2/σ^2 will vary.

[0084] For γ=1/8 it can be verified, that $P_b(e)$ in this case provides an upper bound of true

[0085] BER in the range of BER from 0 to $3 \cdot 10^{-3}$. This choice of γ corresponds roughly to the case of 3-bit-quantization with automatic gain control. The A/D conversion thresholds for a 3-bit conversion are designated 101 in Fig. 2. The digital values are designated 102.

[0086] For practical purposes equation (7) may be simplified to:

$$\ln(P_b(e)) \approx \ln(P_{ud}) + A \qquad (8)$$

[0087] A may be considered to be constant for low error rates. As can be learned from Fig. 4, Equation (8) may be used not only for symbol detectors but also for sequence detectors. In the simulation the results of which are shown in Fig. 4, equation (8) gives a reasonable estimation for the BER in the whole range of the BER from $3 \cdot 10^{-4}$ to $3 \cdot 10^{-1}$. It is to be expected that the value of A would change for a different parameters e.g. SNR. Moreover there might be circumstances in which equation (8) can not be used.

[0088] Fig. 3 and 4 show simulation results of a transmission of about one million bits. The sampling phase was changed in an MLSD receiver. Using about 10^6 bits implies that, in this simulation setup, a BER below 10^{-5} cannot estimated meaningfully because the observation interval is too short.

[0089] These simulations have been performed for optically amplified links i.e. optical signal-to-noise ratio limited transmission for the case of severe chromatic dispersion, 1st order PMD and significant ISI.

[0090] While the present invention is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the present invention to the particular illustrative embodiments disclosed, but rather the described illustrative embodiments merely exemplify the various aspects of the present invention, the scope of which is defined by the appended claims.

Claims

1. A method for a receiver comprising:

    receiving a sequence of symbols;

    characterized in that
    determining (51, 52, 53) an unreliable detection event at which the absolute value of a difference between a first metric (m_{ls}) for a first event minus a second metric m_{lc} for a second event is lower than a predetermined threshold.

2. The method of claim 1, **characterized in that** said first metric monotonously depends on the likelihood that a received symbol (u, 106) said sequence of symbols is a first symbol (u_0, 103) and said second metric monotonously depends on the likelihood that said received symbol (u, 106) is a second symbol (u_1, 104).

3. The method of claim 2, **characterized in that** said first symbol is a logic "0" and said second symbol is a logic "1", said unreliable detection event is determined if said received symbol is within a first range (102); said first range comprising a threshold (Θ, 105) used for discriminating as to whether said received symbol is said first or said second symbol.

4. The method of claim 1, **characterized in that** said sequence of symbols being decoded by a maximum-likelihood-sequence detector (50); said first metric (m_{ls}) being a path metric associated with the most likely path designated survivor and the second metric (m_{lc}) being a metric associated with the second most likely path, designated competitor.

5. The method of one of the claims above, **characterized in that** an unreliable detection event is only determined if a decision is based on said first and second metric and if said decision necessarily leads to at least one bit error if said decision is wrong.

6. The method of claim 4, wherein said maximum-likelihood-sequence detector is a truncation-mode Viterbi detector which enforces a decision after a predetermined number of symbols.

7. The method of claim 4, wherein said maximum-likelihood-sequence detector is a block mode Viterbi detector, wherein the survivor is the finally decided path in a block and the second metric being the metric associated with the second most likely path in said block.

8. The method of one of claims 1 to 7, wherein a first unreliable detection event is defined by a first predetermined threshold (51) for the absolute metric difference and a second unreliable detection event is defined by a second predetermined threshold (52, 53) for the absolute metric difference.

9. The method of one of claims 1 to 8, wherein said first and second metrics are represented by digital values and said first and second metrics are equal (51).

10. The method of one of the preceding claims further comprising:

    counting the unreliable detection events by a counter (54, 55, 56);

    reading the counter value after a first period of time.

11. The method of claim 10, further comprising:

    increasing said first period of time, if said counter value at the end of said first period of time is lower than a first threshold;

    resetting said counter and maintaining said first period of time, if said counter value at the end of said first period of time is greater than said first threshold and smaller than a second threshold; and

    resetting said counter value and decreasing said first period of time, if said counter value at the end of said first period of time is greater than said second threshold.

12. The method of claim 11, further comprising:

setting a demodulator parameter (20, 30, 40) depending on the value read from said counter on the basis of a gradient search.

13. The method of claim 12, **characterized in that** said demodulator parameter is an amplification (20) within the receiver before an analog-to-digital conversion (40).

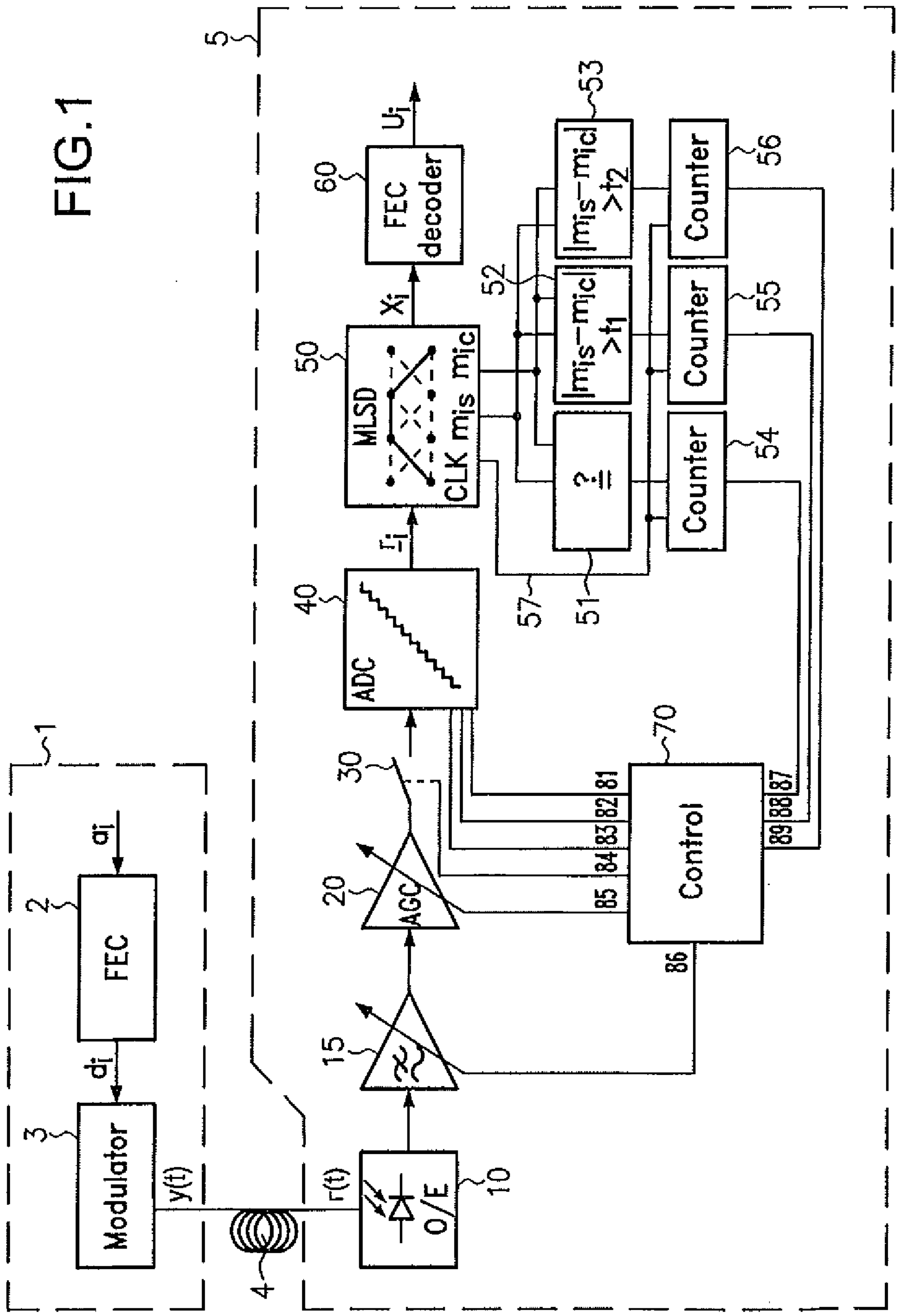
14. The method of claims 12 or 13, **characterized in that** said demodulator parameter is the sampling phase (30), a quantizer bias (81), a non-linearity parameter (83), an upper cut-off frequency of a low-pass filter (15, 86) a residual chromatic dispersion compensation or a phase association.

15. A receiver comprising:

a metric generator (50) for generating a first metric (m_{ls}) for a first event and a second metric (m_{lc}) for a second event,

a unreliability detector (51, 52, 53) for detecting an unreliable detection event when the absolute value of a difference between said first metric minus said second metric is lower than a predetermined threshold.

FIG.1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2
FEC
a_i
d_i
3
Modulator
y(t)
4
r(t)
O/E
10
15
20
AGC
30
ADC
40
r_i
MLSD
CLK m_{is} m_{ic}
50
x_i
FEC decoder
60
u_i
5
$\overset{?}{=}$
51
57
$|m_{is}-m_{ic}|$ $>t_1$
52
$|m_{is}-m_{ic}|$ $>t_2$
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Counter
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Control
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85
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88
89

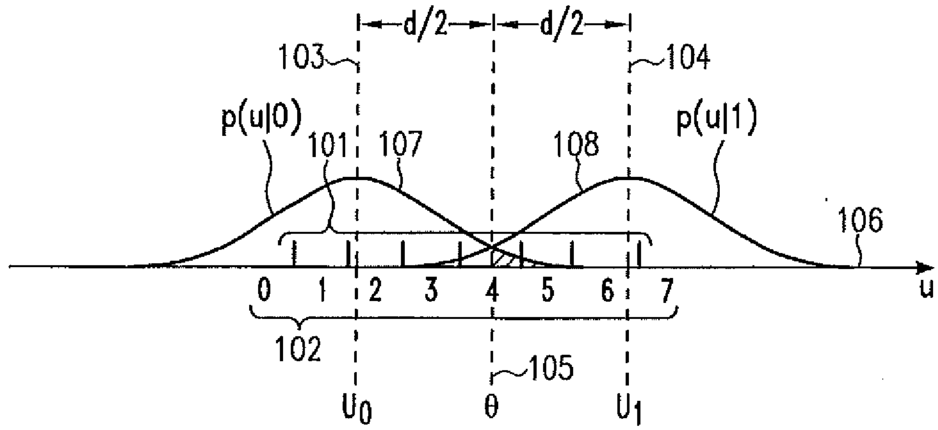
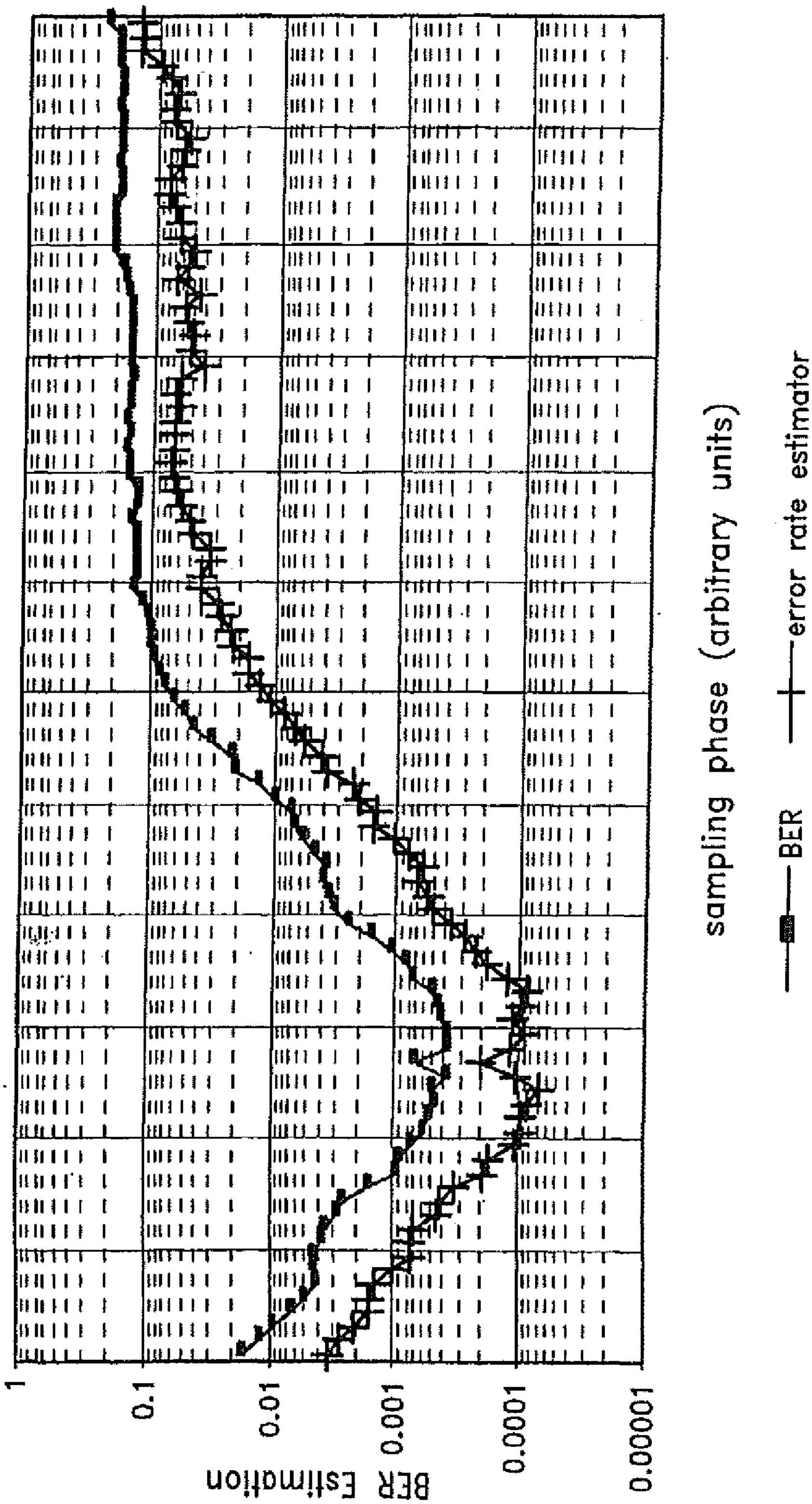


FIG.2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0.01
0.001
0.0001
0.00001
BER Estimation
sampling phase (arbitrary units)
BER
error rate estimator

FIG.3

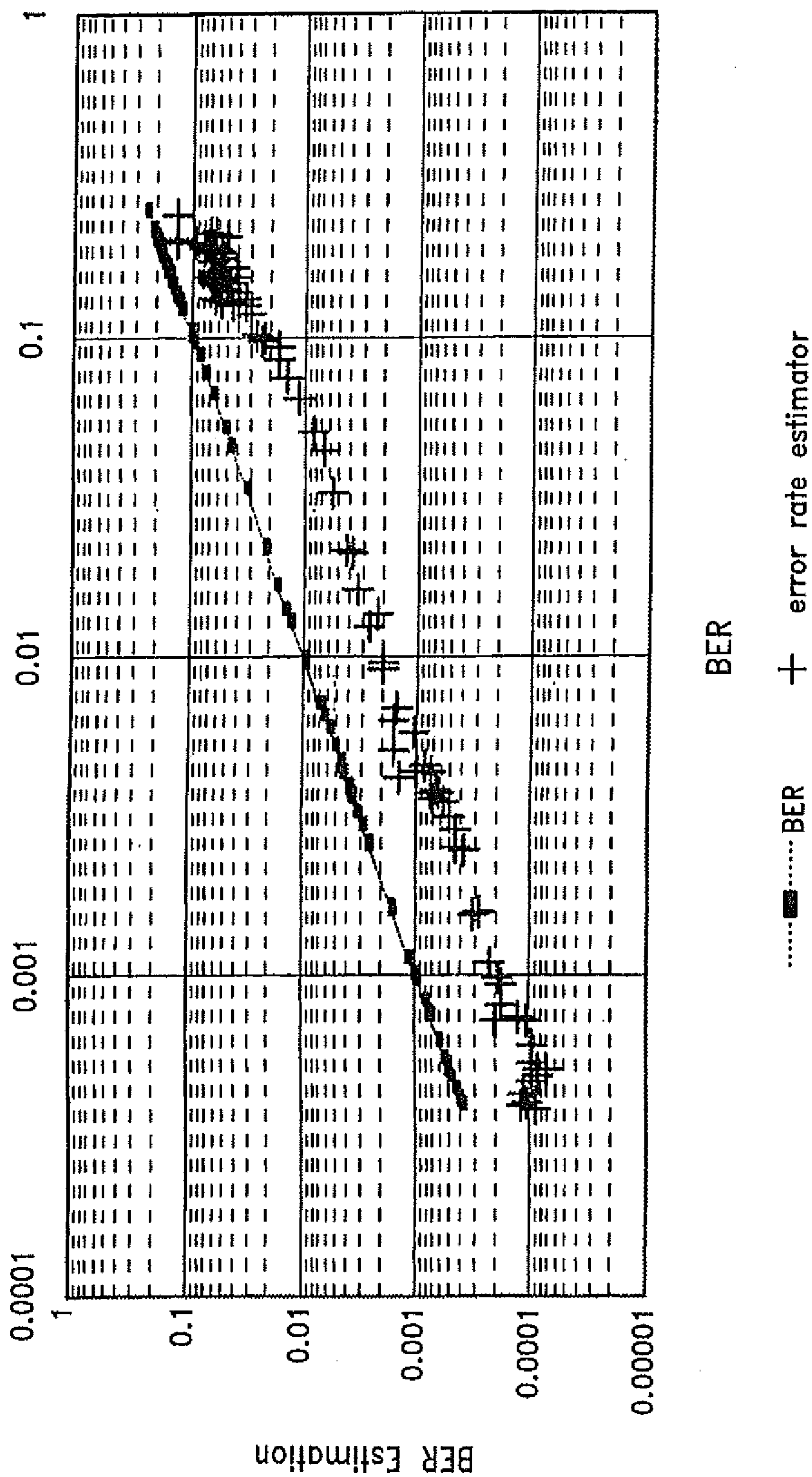
0.0001
0.001
0.01
0.1
1
BER
1
0.1
0.01
0.001
0.0001
0.00001
BER Estimation
BER
error rate estimator

FIG.4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 03 00 2172

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 768 285 A (GRIEP KARL ROBERT ET AL) 16 June 1998 (1998-06-16) * the whole document * ---	1-3,5,8,9,15	H04L1/20 H04L1/00
X	US 5 878 098 A (SCHAFFNER TERRY M ET AL) 2 March 1999 (1999-03-02) * abstract * * column 2, line 16 - column 3, line 51; figures 1-3 * ---	1-3,5,8,9,15	
A	US 6 215 827 B1 (KADABA SRINIVAS R ET AL) 10 April 2001 (2001-04-10) * abstract * * figure 12 * -----	1-15	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 August 2003	Toumpoulidis, T

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 03 00 2172

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15-08-2003

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			BR	9915302 A	24-07-2001
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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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(71) Applicant: **CoreOptics, Inc.,**
c/o The Corporation Trust Center
City of Wilmington, County of New Castle, 19801
Delaware (US)

(72) Inventors:
- **Stojanovic, Nebojsa**
  80469 München (DE)
- **Langenbach, Stefan**
  90409 Nürnberg (DE)

(74) Representative: **Hellmich, Wolfgang, Dr.**
c/o Grünecker, Kinkeldey, Stockmair & Schwanhäusser,
Maximilianstrasse 58
80538 München (DE)

(54) Self-timing method for adjustment of a sampling phase in an oversampling receiver and circuit

(57) This invention discloses a self-timing method for phase adjustment. An analog signal is digitized at a first and second phase with respect to the symbols comprised in an analog signal in order to obtain first and second quantized samples. Then a first counter out of a first plurality of counters is increased if said first quantized value has a first digital value out of a plurality of digital values the first sample may assume and said first counter is associated with the first digital value. Moreover a second counter out of a second plurality of counters is increased if said second quantized samples has a second digital value out of a plurality of possible digital values the second quantized sample may assume and said second counter is associated to said second digital value. Finally the sampling phase is adjusted based on the values of the counters of the first and second plurality of counters. Moreover a digitizing, self-timing circuit is disclosed.

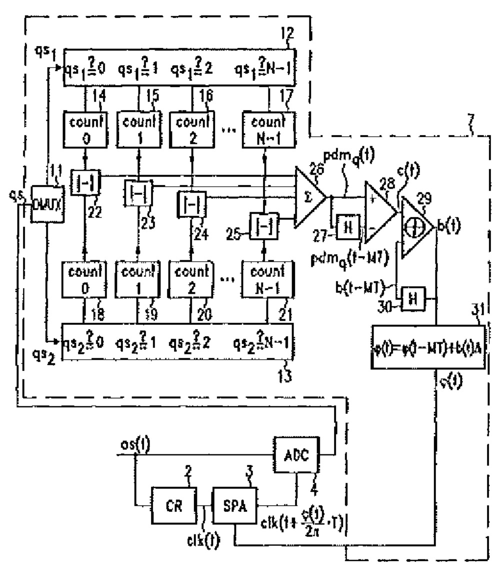

FIG.1a

EP 1 453 238 A1

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Description

[0001] This invention pertains to a self-timing method for phase adjustment of a sampling phase according to the preamble part of claim 1 and a digitizing, self-timing circuit according to the preamble part of claim 7. More specifically this invention relates to a method and a circuit for adjusting the phase of a symbol clock recovered from an analog signal that does not provide a carrier in order to minimize the bit error rate after symbol detection.

[0002] A method of the preamble part of claim 1 and a circuit of the preamble part of claim 7 are described in WO 02/30035 A1 titled "Symbol Timing Recovery Method for Low Resolution Multiple Amplitude Signals".

[0003] **Modern receivers** are used to demodulate, detect and decode digitally transmitted signals e. g. in mobile or fiber optical communications. Due to varying power level of the input signal, an Automatic Gain Control (AGC) circuit is normally included before an Analog-to-Digital Converter (ADC) in order to adapt the signal amplitude to the conversion range. A digital equalizer (EQ) and an error correcting circuit (ECC) usually follow the ADC in order to arrive at an acceptable bit error rate (BER). A clock recovery (CR) circuit extracts frequency and phase and generates a local sampling clock at approximately equidistant points in time, with some more or less fixed phase relation to the transmitted symbol stream. A Sampling Phase Adjustment (SPA) circuit may or may not be present. Its purpose is to add a phase delay to the recovered sampling clock, in order to optimize receiver performance. In simple receivers for low-distortion channels, the SPA is usually missing.

[0004] Various clock recovery schemes are discussed in "Integrated Fiber-Optic Receivers" by A. Buchwald, K. W. Martin, Kluwer Academic Publishers, 1995 (later referred to as "Buchwald95"). The US 5,048,060 titled "Digital Signal Receiving Circuit with Means for Controlling a Baud Rate Sampling Phase by a Power of Sampled Signals" describes a clock recovery method according to which an analog input signal is sampled to produce a series of sampled signals and adjusts the sampling phase based on the series of sampled signals. To this end the sampled signals are equalized and digitally filtered.

[0005] In practical digital communication systems for high-speed transmission and in mobile communications through a band-limited channel, the frequency response of the channel is not known with sufficient precision. Moreover, many channels have a priori unknown and/or time-variant frequency-response characteristics, like, e.g., wireless channels or optical channels. For such channels, it is not possible to design optimum fixed demodulation filters; they require adaptive equalization, instead.

[0006] Channel distortion results in intersymbol interference (ISI), which, when uncompensated, causes high error rate. This calls for receivers with equalizers that can compensate or reduce the ISI in the received signal. There are three well-known types of equalizers: linear equalizer, decision feedback equalizer and maximum-likelihood sequence detector also known as Viterbi detectors (cf. S. U. H. Qureshi, "Adaptive Equalization", Proc. IEEE, vol. 73, 9, pp. 1349-1387, 1985; later referred to as "Qureshi 85").

[0007] In ***symbol rate*** **equalizer structures**, the equalizer taps are spaced at the reciprocal of the symbol rate. When the channel characteristics are unknown, the receiver filter is sometimes matched to the transmitted signal pulse and the sampling time is optimized for this sub-optimal filter. In general, this approach leads to equalizer performance that is very sensitive to the choice of sampling time (cf. J. G. Proakis, "Digital communications", McGraw-Hill, 2001).

[0008] In contrast to the symbol rate equalizer, a ***fractionally spaced equalizer*** (FSE) is based on sampling the incoming signal at least as fast as the Nyquist rate. In general, a digitally implemented fractionally spaced equalizer has tap spacing of mT/n where m and n are integers and $n>m$, and T is the symbol period. Usually, a $T/2$-spaced equalizer is used in many applications. Simulations results demonstrating the effectiveness of the FSE over a symbol rate equalizer have been given in Qureshi 85; G. Ungerboeck, "Fractional tap-spacing equalizer and consequences for clock recovery in data modems", IEEE Trans. Commun., vol. COM-24, pp. 856-864, 1976 and S. U. H. Qureshi and G. D. Jr., Forney, "Performance and properties of a T/2 equalizer", Natl. Telecom. Conf. Record, pp. 11.1.1-11.1.14, Los Angeles, 1977. The authors have shown that the FSE does not exhibit sensitivity to choice of timing phase. However, for severely distorted channels this conclusion is not valid. Hence, timing recovery means for providing an appropriate sampling phase have to be implemented even for a FSE.

[0009] Under the crucial assumption that the received signals are sampled at proper sampling frequency and phase, many techniques are known that are capable of accurately restoring the received signals into original digital signals. Therefore, one of the most important processes in a digital receiver is to accurately restore **symbol** timing in terms of frequency and phase, i.e. to determine the points in time when the received signal should be sampled. In some older systems, a specific carrier corresponding to a sampling frequency was transmitted, providing frequency and phase for sampling. However, most modern systems do not provide a carrier; it is therefore important to accurately recover a symbol timing designated also clock recovery (CR) using only the received signal designated self-timing. Without explicit frequency and phase information being available in the receiver, receiver complexity is increased e.g. due to clock recovery circuits or due to the need for error resilient facilities, like error correction circuits.

[0010] Generally, digital methods for sampling phase adjustment can be divided into two groups: symbol-rate sampling methods and oversampling methods utilizing a clock, which is faster than symbol rate.

[0011] In **Symbol-rate Sampling** methods, data is sampled at symbol rate in order to determine sampling phase based on optimization of some control parameter.

[0012] In US 4,494,242 titled "Timing Recovery in a Baud-Rate Sampled-Data System", timing recovery is based on the recognition that the precursor portion of the response of the channel is relatively invariant and predictable. By selecting a specified threshold point in a small-amplitude region of the precursor portion, a basis is provided for generating accurate bipolar error signals that insure consistent baud-rate sampling of received pulses. A similar approach is disclosed in US 4,959,845 titled "Receiver of a System for Transmitting Data Symbols at a Given Baud-Rate".

[0013] However, the assumption of an invariant and a predictable pulse shape fails in many time-variant channels. In US 5,048,060 titled "Digital Signal Receiving Circuit with Means for Controlling a Baud Rate Sampling Phase by a Power of Sampled Signals", inventors calculate an element of the autocorrelation function of a series of baud rate sampled signals and use its value to find the correct sampling phase. Actually, they choose the sampling phase that either maximizes or minimizes this element of the autocorrelation function. This approach is not applicable in severely distorted channels such as, e.g., optical channels with substantial chromatic dispersion and polarization mode dispersion. For example, it can be shown by simulation results that for special channel conditions the autocorrelation function values R(0) and R(T), where T is a bit period, vary very little with sampling phase. Consequently finding extrema is actually impractical. For other channel conditions, the relevant extremum may even occur at a sampling phase with non-minimal BER. Also, if an (AGC) circuit uses outputs of an ADC for amplification adjustment, the AGC circuit will tend to keep signal power at a constant value and the power measurement cannot be used for timing recovery.

[0014] An interesting method is described in WO 00/19655 titled "Timing Recovery for a High Speed Digital Data Communication System based on Adaptive Equalizer Impulse Response Characteristics". The timing recovery technique is based upon an analysis of the impulse response of the equalizer structure having a feed forward equalizer and a decision feedback equalizer. The filter tap coefficients are analyzed and the sampling phase is adjusted such that a cost function associated with the performance of the equalizer structure is substantially optimized. Unfortunately, for very distorted channels, feed forward equalizers and decision feedback equalizers fail due to their high BER. Rather Viterbi equalizers should be used. Generally, the methods based on symbol rate sampling take a long time for synchronization.

[0015] **Oversampling** methods perform sampling of the received signal at a sampling frequency higher than symbol frequency.

[0016] US 5,291,523 titled " Viterbi Receiver with Improved Timing Means" teaches to use two Viterbi detectors and sample the received signal twice in each symbol period.

[0017] In accordance with the disclosure of EP 1 009 125 A2 titled "Viterbi Receiver With Improved Timing Means", synchronization with the received high-speed serial digital signal can be established at high-speed, and synchronization can be adjusted towards the zero transition point of the received signal. Fig. 3 of EP 1 009 125 A2 illustrates four-fold over-sampling.

[0018] A received symbol stream is M-fold and 12-fold oversampled and correlated with a known synchronization word in US 5,533,066 ("Apparatus and Method for Estimating Maximum Likelihood Sequence Using Optimum Sampling Phase") and WO 02/076010 A2 ("Symbol Recovery From an Oversampled Hard-Decision Binary Stream"), respectively. However, usage of a synchronization word is undesirable in many applications. Moreover, the main weakness of techniques using massive oversampling is the required high processing speed. N-fold oversampling necessitates processing at a frequency N times higher than symbol frequency. This is not feasible in high-speed systems such as 10 GHz or 40 GHz optical systems.

[0019] In WO 02/30035 A1 the inventors describe symbol timing in a system which does not provide a carrier corresponding to a symbol frequency. By collecting a histogram of samples for a predetermined number of symbol times symbol edges and a maximum eye opening are determined. Specifically an average, weighted average, or other method is applied to determine an average timing for maximum eye opening for each symbol time. Eight-fold over-sampling is employed.

[0020] It is the object of this invention to provide an improved method and an improved sampling phase adjustment circuit.

[0021] This object is achieved by the subject matter of the independent claims.

[0022] Preferred embodiments of the invention are the subject matter of the dependent claims.

[0023] The advantage of choosing a sampling phase so that a population difference parameter is maximized is that this leads to a, at least nearly, optimum, i.e. to a minimized bit error rate. Following the de-facto conventions in the literature, the terms "optimal" or "optimized" are used in a somewhat loose sense. What is meant is that a solution of minimized BER is sought within some practical framework or solution space, not excluding the case that in a slightly modified framework even lower BER might be achieved.

[0024] Provided that the first and second digital values may assume N different digital values, a number of N counters in each of the first and second plurality of counters provides the most accurate approximation of the population difference parameter defined in equation (1).

[0025] A simple and robust algorithm for maximizing the population difference parameter and thereby optimizing the sampling phase in order to arrive at a minimum BER is provided. To this end the sampling phase is increased, if the population difference parameter increases with the sampling phase and decreased otherwise. More specifically, the sampling phase is increased if a second population difference parameter following a first population difference parameter is bigger than the first population difference parameter and the sampling phase has been increased between the first and second population difference parameter. The sampling phase is also increased if the second population difference parameter is smaller than the first population difference parameter and the sampling phase has been decreased between the first and second population difference parameter.

[0026] Using dedicated circuits like counters, absolute difference circuits, de-multiplexer and first and second distribution circuits provide for a high operation speed.

[0027] Since the counters count M quantized samples the necessary operation speed after the counters drops approximately by a factor M wherein M may be chosen to be two thousand. As a consequence general purpose logic circuits like a microprocessor or CPU may be used rather than dedicated logic in order to save development and production costs for low volume batches.

[0028] In order to avoid a delay when a microprocessor or CPU sequentially reads out the counter values holding circuits may be provided between the counters and the microprocessors for temporarily storing the counter values after M samples have been processed. So the holding circuits constitute an interface which insures that all quantized samples are taken into consideration for the calculation of the population difference parameter i.e. no quantized samples are ignored during an idle period after M quantized samples have been processed.

[0029] This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig.1a	shows one embodiment of an inventive sampling phase adjustment circuit;
Fig.1 b	shows a second embodiment of an inventive sampling phase adjustment circuit;
Fig. 2	shows some relevant units of a digital receiver which may be used for high speed optical data transmission; and
Fig. 3	shows the dependence of the bit error rate and a population difference parameter on the sampling phase.

Abbreviations

[0030]

ADC:	Analog-to-digital converter
AGC:	Automatic gain control
BER:	Bit error rate
CPU:	Central processing unit
CR:	clock recovery
ECC:	Error correcting code, error correction circuit
EQ:	digital equalizer
FSE:	Fractionally spaced equalizer
ISI:	intersymbol interference
PS:	phase shift
SPA:	sampling phase adjustment
XOR:	exclusive-OR

Mathematical Symbols

[0031]

b(t):	timing signal
$c\varphi_k(i)$:	counter state of counter i for phase φ_k after M symbols
c(t):	control signal
clk:	clock
n:	resolution in bits of the quantizer
N:	number of counters in each group, number of quantization levels

M: number of symbols counted
pdf: probability density function
pd: population difference parameter
pdm: modified population difference parameter
pd_q: quantized population difference parameter
pdm_q: quantized modified population difference parameter
T: symbol period
Δ: sampling phase adjustment step
φ: phase
φ_1, φ_2: sampling phases

[0032] While the present invention is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the present invention to the particular illustrative embodiments disclosed, but rather the described illustrative embodiments merely exemplify the various aspects of the present invention, the scope of which is defined by the appended claims.

Sampling Phase Adjustment Method

[0033] The sampling phase adjustment (SPA) method exploits sample statistics in order to adjust the sampling instants to their correct value. The sample statistics are obtained from the waveform of a plurality of symbols or pulses at different sampling instants. The SPA method is performed within a receiver of digitally transmitted signals. The relevant parts of the receiver are presented in Fig. 2. The received electrical signal is designated s(t). It may be the output signal of a preamplified antenna signal in the case of mobile communications or the output of a optical-to-electrical interface of an optical receiver. Due to varying power level of the received signal s(t), an Automatic Gain Control (AGC) circuit 1 is included before the Analog-to-Digital Converter (ADC) 4 in order to generate a gain controlled signal gs(t). The AGC circuit 1 ensures a proper analog-to-digital conversion of the analog signals. ADC 4 outputs quantized samples qs. A digital equalizer (EQ) 5 and an error correcting circuit (ECC) 6 usually follow the ADC.

[0034] A clock recovery (CR) circuit 2 extracts frequency and phase and generates a local sampling clock at equidistant points in time, with some fixed phase relation to the transmitted symbol stream. As explained above (cf. Buchwald95), CR circuit 2 may be connected to the output of the AGC 1 in order to recover the clock on the bases of the gain controlled signal gs(t). Alternatively or in addition the CR circuit 2 may be connected via CR logic circuit 8 to the output of ADC 4 in order to recover the clock on the basis of the quantized samples (cf. US 5,048,060).

[0035] A Sampling Phase Adjustment (SPA) circuit 3 adds a phase delay to the recovered sampling clock, in order to optimize receiver performance. The phase delay is determined by SPA logic circuit 7 based on the quantized samples qs. Two embodiments of SPA logic circuit 7 are shown in Fig. 1a and 1b.

[0036] In order to reduce the bit error rate (BER) at the output of equalizer 5, which is implemented as Viterbi equalizer in one embodiment, the signal is oversampled at twice the symbol rate.

[0037] Samples representing the transmitted symbols are processed to get the correct sampling phase. The two samples representing a transmitted symbol are sampled at phase φ_k, k ={1,2}, $0 \leq \varphi_k \leq 2\pi$. To find the best sampling phase a population difference parameter pd defined by equation (1) may be utilized:

$$pd = \int_{-\infty}^{\infty} \left| pdf_{\varphi_1}(x) - pdf_{\varphi_2}(x) \right| dx \qquad (1)$$

pdf denotes the amplitude probability density function at either oversampling phase. pd is called a population difference parameter, because it describes the overall difference in population (density) per possible amplitude level.

[0038] There is no practical way for calculating the values of these probability density functions in real systems. Consequently, these distributions are approximated by their discrete counterparts, i.e. by amplitude histograms obtained from processing quantized samples.

[0039] The ADC 4 has N quantization levels. In an embodiment N is a power of 2: $N=2^n$. In this embodiment n bits are used to represent a sample value. The N different amplitudes are mapped into digital words denoted by a_i, i = {1,2,...,N} , and $a_i = i-1$. For a predetermined duration the timing recovery circuit counts the occurrences of each possible word at the two different sampling instants φ_k, k ={1,2} by using 2N counters. By applying this counting, two histograms approximating the probability density functions are obtained. The counter states after M symbols are denoted $c\varphi_k(i)$.

A quantized population difference parameter pdq is defined in equation (2):

$$pd_q = \sum_{i=0}^{N-1} \left| \frac{c_{\varphi 1}(i)}{M} - \frac{c_{\varphi 2}(i)}{M} \right| \tag{2}$$

$$\sum_{i=0}^{N-1} c_{\varphi k}(i) = M \text{ for k=\{1,2\}} \tag{3}$$

[0040] The sum of all counter states $C\varphi_k(i)$ after M symbols is M as indicated by equation (3). For reasons of practical implementation, we introduce a quantized modified population difference parameter pdmq:

$$pdm_q = \sum_{i=0}^{N-1} \left| c_{\varphi 1}(i) - c_{\varphi 2}(i) \right| = M \cdot pd_q \tag{4}$$

Implementation

[0041] An embodiment of the SPA logic circuit 7 for calculating pdmq and timing adjustment is shown in Fig. 1a. It comprises a de-multiplexer 11, distribution circuits 12 and 13, counters 14, 15, 16, 17, 18, 19, 20 and 21, absolute difference circuits 22, 23, 24 and 25, adder 26, a holding circuit 27, a comparator 28, an exclusive-OR (XOR) circuit 29 and a phase calculation circuit 31 . The quantized samples qs are first demultiplexed by demultiplexer 11. The quantized samples qs_1 which have been sampled at phase φ_1 are provided to distribution circuit 12 by demultiplexer 11. On the other hand quantized samples qs_2 sampled at phase φ_2 are provided to distribution circuit 13 by demultiplexer 11. The distribution circuits compare each quantized sample to a plurality of digital values the quantized samples may assume. To each of the digital values a counter is associated. The distribution circuit generates a clock pulse for every quantized sample it receives in order to increment the counter to which the digital value of the quantized sample is associated with. Thereafter the 2N counters 14 to 21 count all events during a predetermined time period MT, where T is the symbol period. The absolute difference circuits 22 to 25 and the adder 26 implement equation (4) i. e. calculate the $pdm_q(t)$ parameter value at time t.

[0042] In another embodiment the ADC 4 may already have two outputs, a first output for the quantized samples qs_1 which have been sampled at phase φ_1 and a second output for the quantized samples qs_2 which have been sampled at phase φ_2. This embodiment does not comprise demultiplexer 11. Rather the first and second outputs are directly connected to the inputs of distribution circuits 12 and 13, respectively.

[0043] A further embodiment comprises a 1:m-type demultiplexer 11, m distribution circuits, m counter groups, each comprising N counters and N/2 absolute difference circuits. Consequently the circuitry between demultiplexer 11 and adder 26 is m-fold parallel. Provided that 2-fold oversampling is employed in this embodiment, the m-fold parallelism decreases the necessary processing speed of the distribution circuits, counters and absolute value circuits by a factor of m/2 compared to the embodiment shown in Fig. 1 a.

[0044] Holding circuit 27 stores the previously calculated $pdm_q(t\text{-}MT)$ parameter value which has been calculated at time t-MT. Comparator 28 compares the newly calculated $pdm_q(t)$ parameter value with the previously calculated $pdm_q(t\text{-}MT)$ parameter value in order to output control signal $c(t) \in \{-1,1\}$. Control signal c(t) is input into XOR circuit 29. XOR circuit 29 generates a timing signal $b(t) \in \{-1,+1\}$ to be used for sampling phase adjustment. Timing signal b(t) is feed back to the other input of XOR circuit 29 via holding circuit 30 in order to delay timing signal b(t) by MT. Consequently the XOR circuit 29 XORs c(t) and b(t-MT). Table 1 depicts its functionality.

Table 1:

functionality of XOR circuit 29		
c(t)	b(t-MT)	b(t)
-1	-1	1

Table 1: (continued)

functionality of XOR circuit 29		
c(t)	b(t-MT)	b(t)
-1	1	-1
1	-1	-1
1	1	1

[0045] Practically, the sampling phase adjustment circuit 3 works in a dithering mode and during an adjustment time this circuit will tend to find the desired sampling phase, that is, the sampling phase maximizing the population difference parameter pdmq.

[0046] The new value of a sampling phase φ(t) is obtained by using equation (5):

$$\varphi(t) = \varphi(t\text{-}MT) + b(t)\Delta \tag{5}$$

[0047] In equation (5) φ(t-MT) represents the previous or old sampling phase and Δ represents a sampling phase adjustment step. Equation (5) is implemented in phase calculation circuit 31. Sampling phase p(t) is provided to SPA circuit 3 which updates the phase shift φ(t) in compliance with equation (5) after a time of MT and shifts the clock clk (t) provided by clock recovery circuit 2 by (φ(t)/2π)T in order to generate a shifted clock clk(t+(φ(t)/2π)T). After a few phase adjustments, the sampling phase providing the maximum value of the pdm_q parameter will be reached, and subsequently be tracked.

[0048] In an alternate embodiment XOR circuit 29 may be a conventional logic circuit inputting either logic 1s or 0s and outputting 0s or 1s. In this embodiment equation 5 must be modified in that previous sampling phase φ(t-MT) is increased by Δ if b(t) is one and old sampling phase is decreased by Δ if b(t) is equivalent to 0 in phase calculation circuit 31.

[0049] Fig. 1 b shows a second embodiment of SPA logic circuit 7. In contrast to the first embodiment shown in Fig. 1a the elements 22 to 31 are replaced by holding circuits 41, 42, 43, 44, 45, 46, 47 and 48, and microprocessor 49. Upon processing M symbols by de-multiplexer 11, distribution circuits 12 and 13 and counters 14 to 21, the counter values are stored in holding circuits 41 to 48. Then the counters are reset and are ready for processing the next 2M samples of the next M symbols. Microprocessor 49 then reads out the values of the holding circuits 41 to 48 and calculates a population difference parameter pd_q or pdm_q in compliance with equations 2 or 4, respectively. Then the microprocessor performs the functionality of holding circuit 27, comparator 28, XOR circuit 29, holding circuit 30 and phase calculation circuit 31 as described in connection with Fig. 1a.

[0050] As will be explained later in connection with the simulation result a typical value for M is 2000. As a consequence the required operating frequency of the multiplexer 11, distribution circuits 12 and 13 and counters 14 to 21 must have a substantially higher operation speed than microprocessor 49. Although microprocessor 49 has to perform more than one operation in order to calculate equation (2) or (4) and perform the maximum search a substantial difference in operation speed of roughly a factor 20 remains for M equivalent to 2000 provided that the processing of the counter values takes 100 microprocessor clock cycles. So even for high speed applications a general-purpose microprocessor 49 having a moderate clock frequency can be used. The application of standard microprocessors reduces development costs and receiver costs especially for small batch sizes.

[0051] The holding circuits 41 to 48 may be omitted if microprocessor 49 is quick enough to enter all counter values within a short time or a certain number of samples are discarded in an idle period between the blocks of M samples which are counted. In the idle period the microprocessor 49 may read out the counter values.

[0052] In another embodiment the counter values are read out by CPU one after another in a distance smaller than MT/(2N). Then each counter value is reset. In this embodiment the periods of time each counter evaluates are shifted with respect to each other. Since it is assumed that the symbols do not appear in a certain pattern but rather are statistically independent this shift may be acceptable.

[0053] In a third embodiment which is not shown in a figure the quantized samples may be directly input into a microprocessor which performs the function of elements 11 to 31 shown in Fig. 1 a. Such a circuit structure can be applied only to moderate transfer rates due to operation speed limitation of the microprocessor 49. In this embodiment counters 14 to 21 may be implemented simply by registers which are increased by an adder logic.

Simulation

[0054] To show the power of the inventive method an optical channel with a high amount of chromatic dispersion, polarization mode dispersion, and noise was simulated. The sampling resolution was T/32 equivalent to 32-fold over-sampling for simulation purposes in order to arrive at a quasi-continuous signal. After ADC 4, a fractionally spaced ML equalizer using two samples in a bit slot for a branch metric calculation was applied. The BER obtained at the output of the fractionally spaced ML equalizer is shown in Fig. 3, where the bit error rate shown at time instant t is obtained by using samples at point t and t+T/2. In Fig. 3 the pdm_q parameter is represented, normalized by its maximum value. It can be seen that sampling at time instants (t_1, t_2) produces a nearly optimum BER performance of 4.10^{-4}. In fact, the true minimum is 4/32T earlier; however, for practical purposes, this deviation from true minimum is not significant. In this connection reference is made to Fig. 2, specifically ECC 6 which can operate at BERs of 10^{-3} and reduces these BERs to 10^{-9} to 10^{-15} at its output. Nearly optimum BER is also obtained for the case of sampling at time instants (t_2, t_3). Sampling at time instants (t_1', t_2') leads to satisfactory BER, which, however, is still significantly worse than the BER produced when sampling at time instants (t_1, t_2).

[0055] In one bit slot there are two local minima and two local maxima of the pdmq parameter. By selecting either of these maxima the equalizer 5 and ECC 6 will have almost minimum BER at its respective output.

[0056] Auxiliary simulation results indicate that about 2000 symbols are enough to get a sufficiently accurate value of the pdmq parameter for use in sampling phase adjustment.

[0057] Further modifications and variations of the present invention will be apparent to those skilled in the art in view of this description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the present invention. It is to be understood that the forms of the invention shown and described herein are to be taken as the presently preferred embodiments.

Claims

1. A self-timing method for phase adjustment of a sampling phase (CLK) to an analog signal (s(t)) comprising a stream of symbols, the method comprising:

   digitizing (4) the analog signal at a first phase with respect to said symbols in order to obtain a first quantized sample (qs_1) having a first digital value out of a first plurality of digital values;

   digitizing (4) the analog signal at a second phase with respect to said symbols in order to obtain a second quantized sample (qs_2) having a second digital value out of a second plurality of digital values; and

   repeating said digitizing at said first and second phases for different symbols comprised in said analog signal;

   characterized by:

   increasing a first counter out of a first plurality of counters (14, 15, 16, 17); said first counter being associated with said first digital value;

   increasing a second counter out of a second plurality of counters (18, 19, 20, 21); said second counter being associated with said second digital value;

   said repeating further comprises repeating said increasing of said first and second counters;

   adjusting (31) said sampling phase based on the values of said counters of said first and second plurality of counters.

2. The method of claim 1, **characterized in that** a population difference parameter (pdm_q) is calculated based on the values of the counters of said first and second plurality of counters and said sampling phase being adjusted that said population difference parameter is maximized.

3. The method of one of the claims above, **characterized in that** said first and second pluralities of counters comprise N counters each.

4. The method of claim 3, **characterized in that** each counter in said first plurality of counters is associated with a

counter in said second plurality of counters; a population difference parameter is the sum (26) of the absolute values of the differences (22, 23, 24, 25) between the values of said counters of said first plurality of counters and the values of the corresponding counters in said second plurality of counters.

5. The method of one of the claims above, **characterized in that** said first and second plurality of digital values comprise N different values and said first and second pluralities of counters comprise N counters each.

6. The method of claim 2 or claims 3 to 5, as far as they refer to claim 2, characterized further by:

repeatedly calculating said population difference parameter;

comparing (28) a first population difference parameter ($pdm_q(t\text{-}MT)$) to a second population difference parameter ($pdm_q(t)$) following said first population difference parameter;

increasing (31) said sampling phase ($\varphi(t)$), if said second population difference parameter ($pdm_q(t)$) is bigger (28) than said first population difference parameter ($pdm_q(t\text{-}MT)$) and said sampling phase has been increased ($b(t\text{-}MT)$) after the calculation of said first population difference parameter or if said second population difference parameter ($pdm_q(t)$) is smaller than said first population difference parameter ($pdm_q(t\text{-}MT$) and said sampling phase has been decreased ($b(t\text{-}MT)$) after the calculation of said first population difference parameter ($pdm_q(t\text{-}MT)$); and

decreasing said sampling phase ($\varphi(t)$) if said second population difference parameter ($pdm_q(t)$) is smaller (28) than said first population difference parameter ($pdm_q(t\text{-}MT)$) and said sampling phase has been increased after the calculation of said first population difference parameter ($b(t\text{-}MT)$) or if said second population difference parameter is bigger (28) than said first population difference parameter ($pdm_q(t\text{-}MT)$) and said sampling phase has been decreased after the calculation of said first population difference parameter ($pdm_q(t\text{-}MT)$).

7. A digitizing self-timing circuit comprising:

an analog-to-digital converter (4) receiving an analogue signal ($gs(t)$) comprising a stream of symbols; said analog-to-digital counter (4) performing two analog-to-digital conversions per symbol period (T), thereby producing first quantized samples (qs_1) at a first phase and second quantized samples (qs_2) at a second phase; said first quantized samples have digital values out of a first plurality of digital values and said second quantized samples having digital values out of a second plurality of digital values;

characterized by:

a first plurality of counters (14, 15, 16, 17) each counter of said first plurality being associated with a first digital value and being incremented if a first quantized sample (qS_1) is equivalent to said first digital value;

a second plurality of counters (18, 19, 20, 21) each counter of said second plurality being associated with a second digital value and being incremented if a second quantized sample (qs_2) is equivalent to said second digital value; and

a sampling phase adjustment circuit (3) for controlling the sampling times of said analog-to-digital counter (4) based on the values of the counters of said first and second plurality of counters.

8. The circuit of claim 7, further comprising:

circuitry (22, 23, 24, 25, 26) connected to said counters of said first and second plurality of counters calculating a population difference parameter (pdm_q) from the values of the counters of said first and second plurality of counters and a maximizing circuit (27, 28, 29, 30, 31) being connected to said circuitry (22, 23, 24, 25, 26) and said sampling phase adjustment circuit (3) for controlling said sampling phase adjustment circuit in order to maximize said population difference parameter (pdm_q).

9. The circuit of claim 8, each counter of said first plurality of counters being associated to a different one of said second plurality of counters in a one to one relationship, said circuitry comprising:

a plurality of absolute difference circuits (22, 23;24, 25) each absolute difference circuit being connected to a pair of associated counters and calculating the absolute difference between the counter values of said pair of associated counters; and

an adder (26) connected to the outputs of said plurality of absolute difference circuits and said maximizing circuit (27, 28, 29, 30, 31) for summing the absolute differences and providing the sum to said maximizing circuit (27, 28, 29, 30, 31).

10. The circuit claim 7 or 8, said maximizing circuit further comprising:

a comparator circuit (27, 28) for receiving the output of said circuitry (22, 23, 24, 25, 26) and comparing a first population difference parameter (pdm_q(t-MT)) to a second population difference parameter (pdm_q(t)) following said first population difference parameter (pdm_q(t-MT);

a phase calculation circuit (29, 30, 31) connected to the output of said comparator circuit (27, 28) and to said sampling phase adjustment circuit (3) for outputting a phase shift to said sampling phase adjustment circuit (3); said phase calculation circuit (29, 30, 31)

increasing said sampling phase (φ(t)) if said second population difference parameter (pdm_q(t)) is bigger (28) than said first population difference parameter (pdm_q(t-MT)) and said sampling phase has been increased (b(t-MT)) after the calculation of said first population difference parameter or if said second population difference parameter (pdm_q(t)) is smaller than said first population difference parameter (pdm_q(t-MT)) and said sampling phase has been decreased (b(t-MT)) after the calculation of said first population difference parameter (pdm_q(t-MT)); and

decreasing said phase calculation circuit (29, 30, 31) decreasing said sampling phase (φ(t)) if said second population difference parameter (pdm_q(t)) is smaller (28) than said first population difference parameter (pdm_q (t-MT)) and said sampling phase has been increased (b(t-MT)) after the calculation of said first population difference parameter or if said second population difference parameter (pdm_q(t)) is bigger than said first population difference parameter (pdm_q(t-MT)) and said sampling phase has been decreased (b(t-MT)) after the calculation of said first population difference parameter (pdm_q(t-MT)).

11. The circuit of one of claims 7 to 9, further comprising:

a de-multiplexer (11) connected to said analog-to-digital converter (4) for outputting said first quantized samples (qs_1) at a first output and said second quantized samples (qs_2) at a second output;

a first distribution circuit (12) connected to said first output of said de-multiplexer (11) and each of said first plurality of counters; said first distribution circuit comparing a first quantized sample to a plurality of digital values to each of which a counter of said first plurality of counters (14, 15, 16, 17) is associated and generating a clock pulse to increment the counter to which the digital value is associated which is equivalent to said first quantized sample; and

a second distribution circuit (13) connected to said second output of said de-multiplexer (11) and each of said first plurality of counters; said second distribution circuit comparing a second quantized sample to a plurality of digital values to each of which a counter of said second plurality of counters (18, 19, 20, 21) is associated and generating a clock pulse to increment the counter to which the digital value is associated which is equivalent to said second quantized sample.

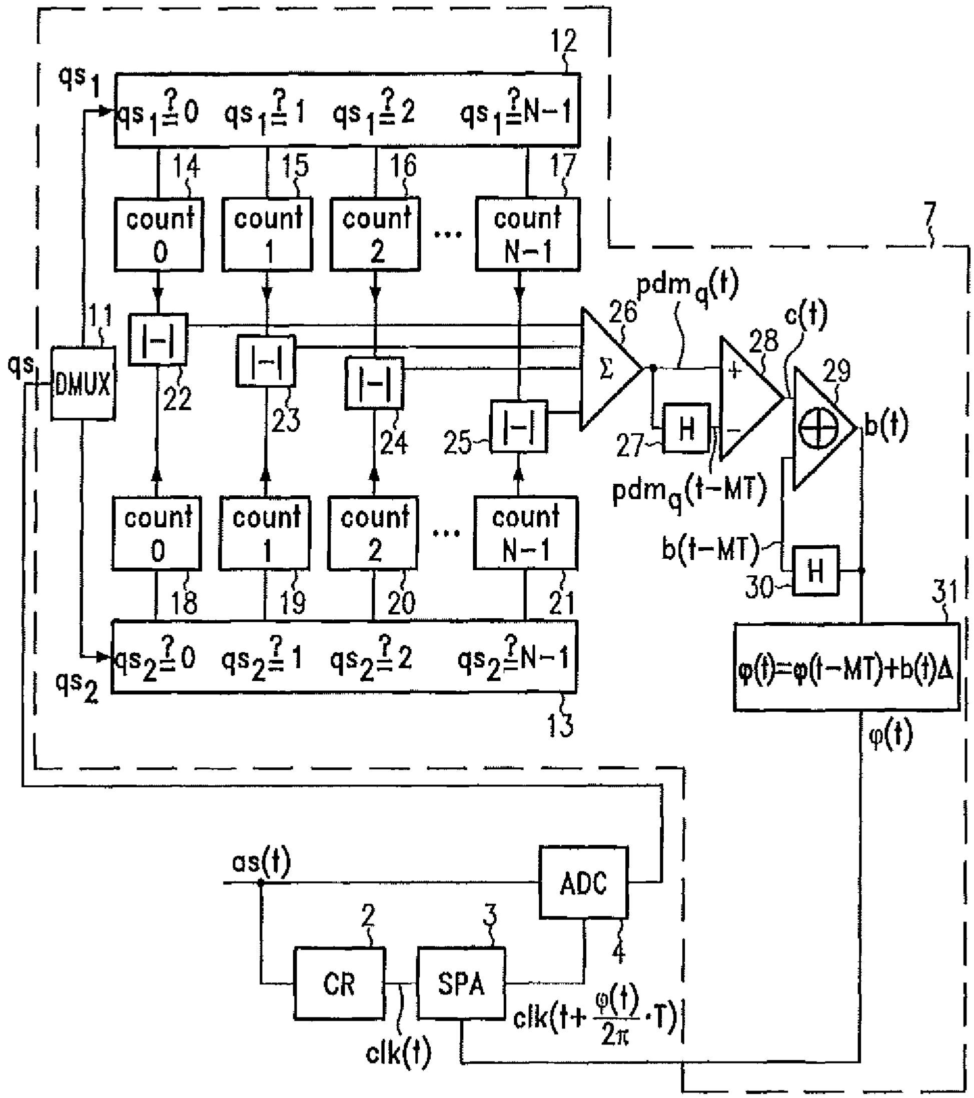
12
qs1
qs1 ?= 0 qs1 ?= 1 qs1 ?= 2 qs1 ?= N−1
14 15 16 17
count 0
count 1
count 2
count N−1
7
pdmq(t)
26
c(t)
28
29
11
qs
DMUX
Σ
+
−
b(t)
22 23 24 25
27
H
pdmq(t−MT)
b(t−MT)
30
H
count 0
count 1
count 2
count N−1
18 19 20 21
31
qs2 ?= 0 qs2 ?= 1 qs2 ?= 2 qs2 ?= N−1
φ(t)=φ(t−MT)+b(t)Δ
qs2
13
φ(t)
as(t)
ADC
2 3
4
CR
SPA
clk(t+ φ(t)/2π ·T)
clk(t)

FIG.1a

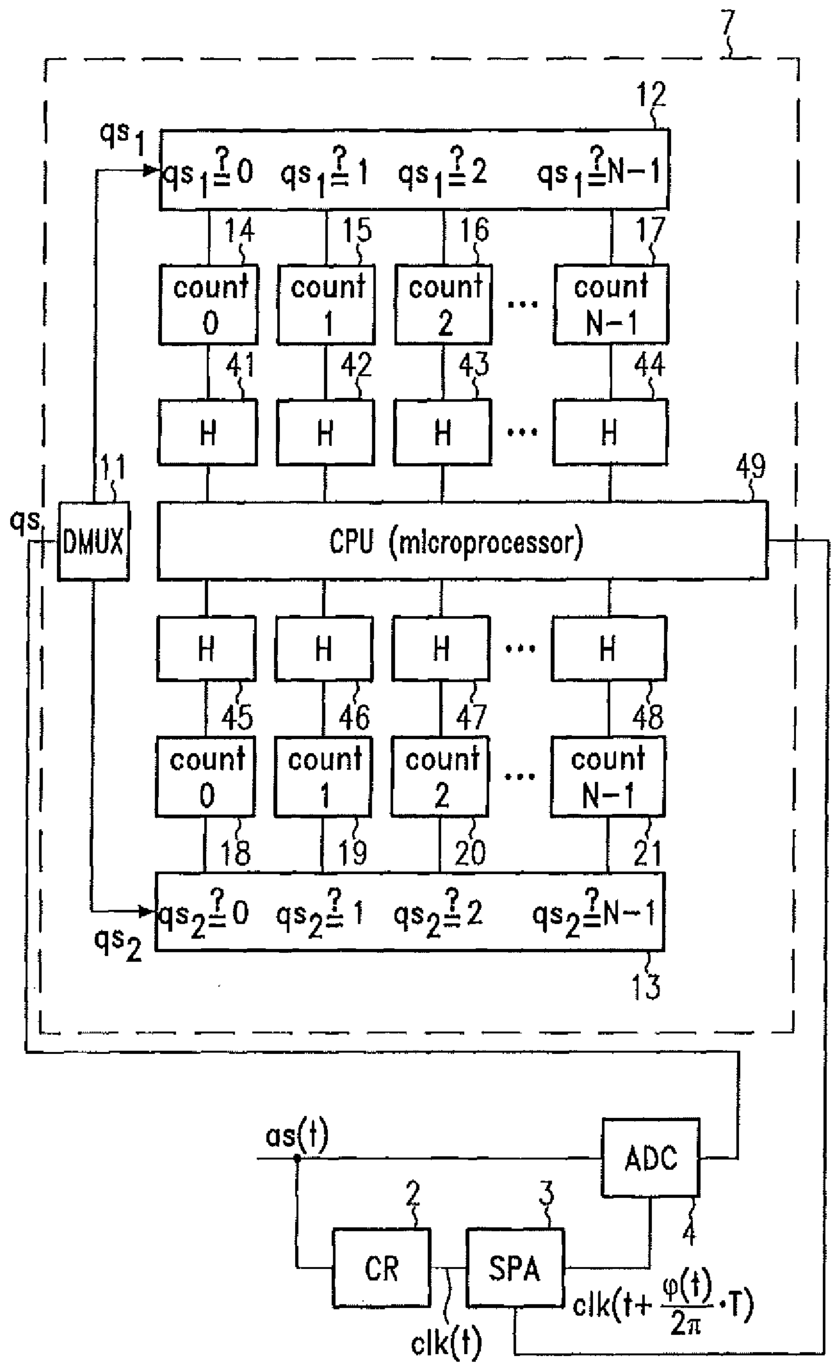
7
12
qs1
qs1 ?= 0
qs1 ?= 1
qs1 ?= 2
qs1 ?= N−1
14
15
16
17
count 0
count 1
count 2
count N−1
41
42
43
44
H
H
H
H
11
49
qs
DMUX
CPU (microprocessor)
H
H
H
H
45
46
47
48
count 0
count 1
count 2
count N−1
18
19
20
21
qs2 ?= 0
qs2 ?= 1
qs2 ?= 2
qs2 ?= N−1
qs2
13
as(t)
ADC
2
3
4
CR
SPA
clk(t+ φ(t)/2π ·T)
clk(t)

FIG.1b

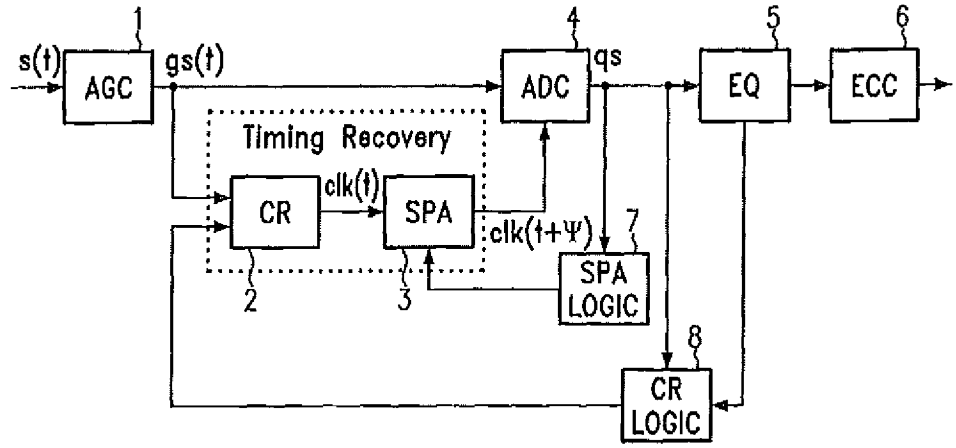
s(t)
AGC
gs(t)
1
ADC
4
qs
EQ
5
ECC
6
Timing Recovery
CR
clk(t)
SPA
clk(t+Ψ)
SPA LOGIC
7
2
3
CR LOGIC
8

FIG.2

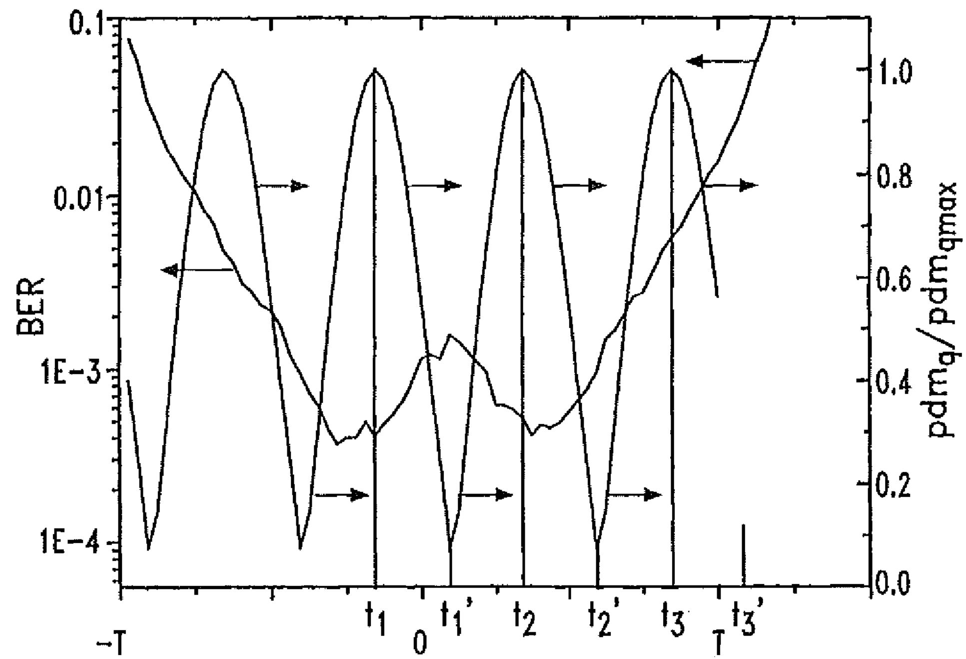
0.1
0.01
1E-3
1E-4
BER
1.0
0.8
0.6
0.4
0.2
0.0
pdm_q/pdm_qmax
-T
t1
0
t1'
t2
t2'
t3
T
t3'

FIG.3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 03 00 4079

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	28 July 2003	Schiffer, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 03 00 4079

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28-07-2003

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(71) Applicant: CoreOptics, Inc.,
c/o The Corporation Trust Center
City of Wilmington, County of New Castle, 19801
Delaware (US)

(72) Inventors:
- Stojanovic, Nebojsa, Prof., Dr.
80469 München (DE)
- Langenbach, Stephan
90409 Nürnberg (DE)

(74) Representative: Hellmich, Wolfgang, Dr.-Ing.
European Patent and Trademark Attorney
Ernsbergerstrasse 14
81241 München (DE)

(54) **Method and circuit for controlling amplification**

(57) This invention relates to a method for controlling an amplification within a receiver. The gain of a variable gain amplifier which amplifies an input signal to obtain a gain-controlled signal is set. Said gain controlled signal is analog-to-digital converted. Thereby digital words are generated. Each digital word has a value out of a plurality of possible digital values. Digital words having a value within a first and a second subset of the possible digital values are counted in order to generate a first and a second counter value. The gain is set in accordance with the first and second counter values in a fashion that all counter values are as equal as possible. Furthermore, this invention is related to a circuit to be used within a receiver for adjusting the gain of a variable gain amplifier in order to ensure a proper analog-to-digital conversion.

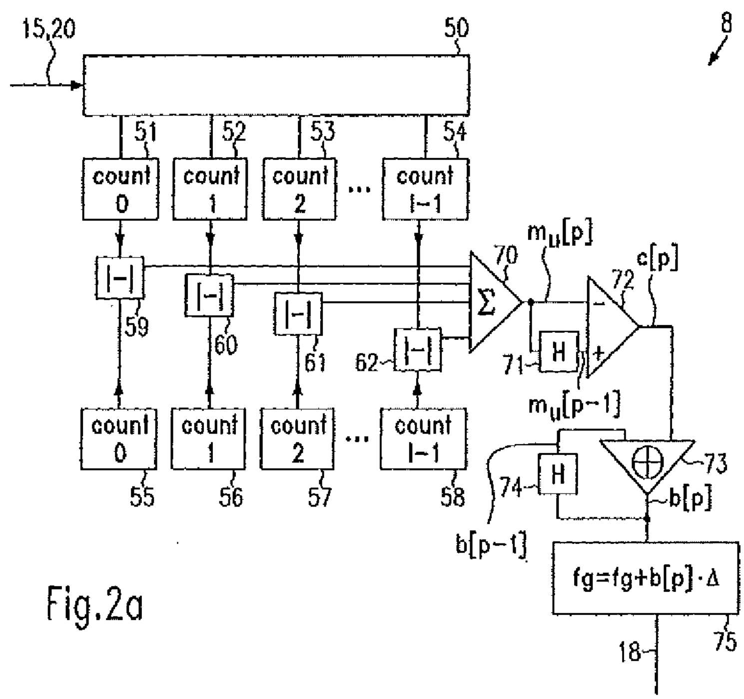

Fig.2a

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Description

[0001] The present invention relates to a method and a circuit according to the preamble parts of claims 1 and 6, respectively. In particular the invention relates to the automatic gain control in digital receivers e.g. for optical data transmission.

[0002] Such a method and circuit are described in US 3,931,584 titled "AUTOMATIC GAIN CONTROL".

[0003] Communication systems are designed to provide reliable transmission of information, whereby they should be able to combat various channel imperfections. In digital communication systems, the most important parameter for the signal quality measurement surely is BER (bit error rate). The signal at the receiver end contains the data and clock information to be extracted. The amplitude of the received signal is attenuated, whereby the attenuation depends on length and type of the transmission channel. Due to varying power level of both wired and wireless digital transmitted signals, an automatic gain control circuit (AGC) is customary placed before a CDR (clock and data recovery) circuit, which comprises a clock recovery circuit (CR), an analog-to-digital converter (ADC) and a sampling circuit, which receives the recovered clock from the clock recovery circuit.

[0004] Automatic gain control is widely employed to adjust the amplification of an input signal in such a way that an output signal has a substantially constant signal level in terms of root mean square, mean or peak values. Most digital communication systems must accommodate received signal levels varying within a range of some tens of dB. However, the power level variation of the AGC output signal should be as low as possible and at least within a range of less than one dB.

[0005] In US 3,931,584 inventors present an AGC separated in two circuits one for coarse and the other for fine gain control. In order to adjust the amplification of the fine AGC, the sign and most significant bit in a digital word that an ADC circuit produces are monitored. An exclusive-OR (XOR) operation is performed on the sign and most significant bit in order to detect zero-one and one-zero combinations which indicate high positive and low negative values in a two's compliment system. Then the zero-one and one-zero combinations are counted within a period of time. According to this document it will be apparent to those skilled in the art that any combination of the digits can be counted to control the amplification of the AGC. A comparator compares the count with a threshold value. If the count is less than the threshold value the fine AGC increases the power level and vice versa. Thereby amplification of the input signal is set to a level that the highest and lowest digital words approach the maximum and minimum, respectively, level expressible by the digital words. So the quantization noise of the converter is reduced by maximizing the number of digital words that are available to express the signal amplitude.

[0006] This method has the shortcomings that the threshold value depends on the communication channel conditions such as noise power, noise distribution, dispersion etc. In case of very distorted channels like wavelength division multiplexing (WDM) or wireless channels the conventional methods might provide sub-optimal or even very bad performance. In time-variant channels, the measurement of channel performance and selection of new thresholds for obtaining optimal decoding performance increase the AGC circuit complexity. These measurements are hardly feasible for very distorted channels. The receiver developed for such channels have to utilize either a channel equalizer or strong ECC (error correcting code) or a combination thereof.

[0007] It is the object of this invention to present a method and circuit for controlling amplification within a receiver in order to arrive at an optimized BER.

[0008] This object is achieved by the subject matter of the independent claims.

[0009] Preferred embodiments of the invention are the subject matters of the dependent claims.

[0010] Following the de-facto conventions in the literature the terms "optimal" or "optimized" are used in a somewhat loose sense. What is meant is that a solution of minimized BER is sought within some practical framework or solution space, not excluding the case that in a slightly modified framework even lower BER might be achieved.

[0011] Grouping more than one possible digital value into subsets advantageously reduces the number of counters required and consequently reduces circuit complexity.

[0012] Minimizing a uniformity parameter provides an efficient method for adjusting the amplification to achieve a close to minimum BER even for highly distorted, time-variant signals. This technique can be applied to non-Gaussian time-variant channels in the presence of linear and nonlinear distortion.

[0013] Defining a first, inner subset and a second, outer subset and comparing the counter values of the inner and outer subsets avoid a minimum search. The amplification is increased if the inner subset is greater than the counter value of the outer subset.

[0014] The difference of the counter value of the inner subset minus the counter value of the outer subset constitutes a control parameter, which can be advantageously used together with popular control algorithms like a proportional-plus-integral-plus-derivative controller (PID controller) or fuzzy controllers.

[0015] In the following preferred embodiments of this invention are described referring to the accompanying drawings.

[0016] Figure 1 shows a block diagram of the relevant units of a receiver according to this invention.

[0017] Figure 2a shows a detailed block diagram of a first embodiment of the fine logic unit.

[0018] Figure 2b shows a detailed block diagram of a second embodiment of the fine logic unit.
[0019] Figure 3 shows a statistic of digitized sample values.
[0020] Figure 4 illustrates counter values for the statistics of figure 3 for a first subset.
[0021] Figure 5 illustrates counter values for the statistics of figure 3 for a second subset.
[0022] Figure 6 shows simulation results.

Abbreviations

[0023]

ADC:	analog-to-digital converter
AGC:	automatic gain control
BER:	Bit error rate
CDR:	clock and data recovery
CR:	clock recovery
ISI:	intersymbol interference
WDM:	wavelength division multiplexing
XOR:	exclusive-OR
ECC:	Error correcting code, error correction circuit
EQ:	digital equalizer
MLSE:	Maximum-likelihood sequence estimator
VGA:	variable gain amplifier

Mathematical Symbols

[0024]

a_i:	digital word
b_j:	quantized sample at time j
c_q:	count of subset S_q
f:	symbol rate
fg:	fine gain control signal
i:	digital word index, $1 \leq i \leq 2^n$
j:	time index, $1 \leq j \leq M$
M:	number of samples
k_q:	expected number of samples in subset S_q
l:	number of subsets
m_c:	coarse gain parameter
m_u:	uniformity parameter
n:	ADC resolution in bit
p:	index for uniformity parameters m_u
q:	subset index, $1 \leq q \leq l$
S:	complete set
S_c:	coarse gain subset
S_q:	subset
t:	time
T:	period sample
T_i:	idle period

[0025] While the present invention is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the present invention to the particular illustrative embodiments disclosed, but rather the described illustrative embodiments merely exemplify the various aspects of the present invention, the scope of which is defined by the appended claims.
[0026] Several counters are introduced, some used for the coarse AGC unit and some others used for fine AGC adjustment, as described in the following.
[0027] Since the gains of the coarse and fine AGC units are controlled by other elements it may be more appropriate

to designate these units as variable gain amplifiers (VGA). AGC and VGA will be used synonymously in the following.

Implementation

[0028] An excellent AGC capability can be realized by using several AGC units. Typically a coarse AGC unit has a wider dynamic rage than a fine AGC unit, which provides for a more accurate gain control. In one embodiment, the coarse AGC unit is controlled in accordance with conventional practice. A peak detector detects either only positive peaks or positive and negative peaks in the output signal of the coarse AGC unit and adjusts its amplification accordingly. In particular it is detected when that the output signal of the coarse AGC unit exceeds a positive threshold or exceeds the positive threshold and falls below a negative threshold for a predetermined portion of time.

[0029] In another embodiment, which is described in connection with Fig. 1, the coarse AGC unit can also be controlled by signal generated in a logic unit or a DSP (digital signal processing) circuit. At start-up, the coarse AGC unit can quickly bring a total gain into working regime and after that the fine AGC would adjust finally the gain providing the minimum BER at the output of the digital equalizer or other decoding circuit.

[0030] More specifically, after power-up the gain of the fine AGC is set to some relaxed initial value, which is an intermediate gain value that is neither close to the maximum nor to the minimum gain of the fine AGC unit in order to allow positive and negative gain adjustments. Then, in an coarse adjustment phase only the gain of the coarse AGC unit is adjusted to bring the input signal of the following ADC into the working regime i. e. a coarse gain parameter m_c remains above some lower threshold. When the input signal has reached the working regime, the gain of the coarse AGC unit remains fixed whereas the gain of the fine AGC unit optimizes the level of the input signal to arrive at a minimum BER during normal operation. The receiver may reenter into the coarse adjustment phase in order to re-adjust the coarse AGC unit, when the gain of the fine AGC unit reaches either its maximum or minimum. During the coarse adjustment phase the gain of the coarse AGC unit is adjusted in such a way that a coarse gain parameter m_c always remains above some lower threshold. The most difficult situation expected in an optically amplified DWDM system is when many channels are switched-away or are added at the same time in an optical add/drop multiplexer (ADM) which causes large power transients in optical amplifiers. When re-entering into the coarse adjustment phase, the gain of the fine AGC is again set to its relaxed initial value and the gain of the coarse AGC unit is adjusted to bring the total gain into the working regime as explained above.

[0031] Figure 1 shows a block diagram of the relevant units of a receiver according to this invention. It comprises a coarse VGA unit 2, a fine VGA unit 3, a clock recovery (CR) 4, a sampler 5, an ADC 6, an digital equalizer 7 and a fine logic unit 8 and a coarse logic unit 9. The input signal 10 that is input into the coarse VGA unit 2 represents the transmitted signal as distorted by the channel at the receiver end. It may be the output signal of an antenna in the case of radio communication or the output signal from an optical-to-electrical interface in the case of optical data transmission.

[0032] The signal at the input of the clock recovery circuit 4 must be strong enough. However, it is even more critical to provide sampler 5 and ADC 6 with a signal having optimal strength in order to arrive at a minimum BER. To this end coarse and fine VGA 2 and 3 amplify the input signal and generate a gain controlled signal 12 which is input into CR circuit 4 and sampler 5. CR circuit 4 recovers the symbol clock and provides control signals on lines 13 and 11 to sampler 5 and ADC 6. These control signals already have an appropriate phase relation to the gain-controlled signal 12. Such clock recovery circuits are described in "Integrated Fiber-Optic Receivers" by A. Buchwald, K. W. Martin, Kluwer Academic Publishers, 1995. It is noted that ADC 6 and sampler 5 could be reversed in sequence.

[0033] The sampler 5 essentially comprises a sample-and-hold circuit, which samples the gain-controlled signal 12 at appropriate points in time and outputs a constant signal on line 14 to the ADC until the next sampling is performed. The ADC provides its output in form of digital words on line 15 to digital equalizer 7 and fine and coarse logic unit 8 and 9. The digital equalizer 7 preferably combats ISI and consequently provides equalizer functionality. The fine logic unit 8 essentially calculates statistics of the digital words provided by the ADC 6 and generates a fine gain control signal on line 18 to control the gain of fine VGA 3. The coarse logic unit 9 operates in a similar fashion and generates a coarse gain control signal on line 19 to control the gain of coarse VGA 2. The operation of the coarse and fine logic unit 8 and 9 will be explained in more detail below. Two embodiments of fine logic unit 8 are shown in figures 2a and 2b.

[0034] In another embodiment sampler 5 and ADC 6 may perform over-sampling. As a consequence, more than one digital words are provided on line 15 for each symbol comprised in the input signal 10. In this case, digital equalizer 7 may reduce the over-sampled digital words to one digital word per symbol and provide this data on line 20 to logic units 8 and 9 or alternatively the over-sampled digital words may be processed directly by the logic units.

[0035] ADC 6 has 2^n quantization levels, where each sample is represented by n bit. The 2^n different quantization levels are mapped into a set S of digital words, denoted by $S=\{a_i\}$, i=1, 2, ... , 2^n. Let the subscript i of the digital word a_i represent the amplitude level of the quantized sample in value order, i.e. $a_1<a_2<...<a_{2^n}$.

[0036] In a particular interval of time MT the DSP counts the occurrences of each possible word, by using 2^n counters. Here M is the number of all words in this interval and T is the symbol period being the reciprocal of the symbol rate of

transmission, f.

[0037] For counting samples of certain amplitude a simple indicator (counting) function defined by equation (1) is used:

$$\delta_a(x)=\begin{cases}1 & , \; x=a \\ 0 & , \; x\neq a\end{cases} \tag{1}$$

[0038] The coarse AGC utilizes a coarse gain parameter m_c indicating the amplified output signal strength. For this purpose, we introduce a subset S_c of S, representing the set of digital words or quantizer levels that are relevant for indicating signal strength. This parameter m_c is obtained by equation (2):

$$m_c = \sum_{a_j \in S_c} \sum_{j=1}^{M} \delta_{a_j}(b_j) \tag{2}$$

b_j is the quantized sample at discrete time index j. For many channels a good choice is to use $S_c=\{a_{2^n}\}$. In contrast, for optical channels or generally for binary channels with signal-dependent noise $S_c=\{a_1,a_{2^n}\}$ provides satisfactory performance. Note that the latter choice can also be applied for other channels, without loss in performance.

[0039] During any coarse adjustment phase the coarse logic unit 9 compares the parameter m_c with one or more thresholds and generates a signal for reducing or increasing the coarse gain accordingly. Consequently, the coarse AGC ensures that the signal has sufficient power, in the specified limits.

[0040] The fine AGC 2 will be adjusted by a uniformity parameter m_u, indicating the uniformity of the distribution of discrete amplitudes. To this end the set *S* of all quantization levels is partitioned into I disjoint subsets (equation (3)), with $2 \leq I \leq 2^n$:

$$S = S_1 \cup S_2 \cup ... S_I \tag{3}$$

[0041] To each subset S_q an integer number k_q is associated. k_q represents the expected number of times a quantization level in the subset S_q will be expected in M observations or samples. Since each sample is associated with exactly one subset equation (4) holds:

$$\sum_{q=1}^{I} k_q = M \tag{4}$$

[0042] Normally, to achieve uniformity, k_q should be chosen as M/I. With additional knowledge about the channel, better performance may possibly be achieved with a slightly non-uniform choice of values k_q.

[0043] The uniformity parameter m_u, controlling the fine AGC unit, is defined by equation (5):

$$m_u = \sum_{q=1}^{I} \left| \left(\sum_{a_j \in S_q} \sum_{j=1}^{M} \delta_{a_j}(b_j) \right) - k_q \right| \tag{5}$$

[0044] With suitable selection of parameters, in particular k_q, minimum BER can be achieved by minimizing the uniformity parameter m_u. An inappropriate selection of parameters can lead to local minima, which make it hard to find the best gain value, producing the lowest number of errors.

[0045] Figure 2a shows a possible implementation of fine logic unit 8. Figure 2a shows a distribution circuit 50, counters 51 to 54, absolute difference circuits 59 to 62, registers 55 to 58, adder 70, comparator 72, holding circuits 71 and 74, exclusive-OR (XOR) gate 73 and fine gain calculation circuit 75. The digital words provided by ADC 6 on line 15 or digital equalizer on line 20 are input into distribution circuit 50. Distribution circuit 50 compares each digital word to a plurality of digital values the digital words may assume in order to associate each digital word to one of the subsets S_q, $1 \leq q \leq 1$. To each of the subsets S_q one of the counters 51 to 54 is associated. Distribution circuit 50 generates a clock pulse for every digital word it receives in order to increment the counter associated with the subset to which the digital word belongs. Additionally, for each subset one absolute difference circuit and one register is provided. Each of the absolute difference circuits calculates the absolute value of the difference of the counter value minus the register value of the counter and the register to which the absolute different circuit is connected to. In each of the registers one number k_q, $1 \leq q \leq l$ is stored. Adder 70 adds the outputs of all absolute different circuits. Consequently, distribution circuit 50, counters 51 to 54, absolute difference circuits 59 to 62, registers 55 to 58 and adder 70 implement equation (5). Therefore, the output of adder 70 constitutes the uniformity parameter m_u.

[0046] The counters 51 to 54 count M digital words input into distribution circuit 50 during a period of MT wherein T is the symbol period. Then a uniformity parameter $m_u[p]$ is calculated at time t_p and the counters are reset.

[0047] Holding circuit 71 stores the previously calculated uniformity parameter $m_u[p-1]$ which has been calculated at time $t_{p-1}=t_p$-MT wherein t_p is the present time. In addition, the calculation of the uniformity parameter m_u may take some idle time T_i during which digital words are ignored on lines 15 or 20. If T_i is different from 0, T_i must be added to MT but, for simplicity, it is assumed to be 0 in the following discussion. Comparator 72 compares the newly calculated uniformity parameter $m_u[p]$ with the previously calculated uniformity parameter $m_u[p-1]$ in order to output control signal $c[p] \in \{-1,1\}$. Control signal c[p] is input into XOR circuit 73. It generates a timing signal $b[p] \in \{-1,+1\}$ to be used for gain phase adjustment. Timing signal b[p] is feed back to the other input of XOR circuit 73 via holding circuit 74 in order to delay timing signal b[p] by MT. Consequently the XOR circuit 73 XORs c[p] and b[p-1]. Table 1 depicts its functionality.

Table 1:

functionality of XOR circuit 73		
c[p]	b[p-1]	b[p]
- 1	-1	1
- 1	1	-1
1	-1	-1
1	1	1

[0048] Practically, minimizing the uniformity parameter m_u and consequently the gain adjustment works in a dithering mode. During operation this circuit adjusts the gain in a way that the uniformity parameter m_u dithers around its minimum.

[0049] The new value of the fine gain control signal is obtained by using equation (6):

$$fg[p] = fg[p-1] + b[p]\Delta \tag{6}$$

[0050] In equation (6) fg[p-1] represents the previous or old fine gain control signal and Δ represents an adjustment step of the fine gain control signal. Equation (6) is implemented in fine gain calculation circuit 75. The fine gain control signal fg is provided via line 18 to fine VGA 3 which updates the gain. After some fine gain adjustments, the gain range will be reached, and subsequently tracked, which corresponds to the minimum uniformity parameter m_u and BER.

[0051] In an alternate embodiment XOR circuit 73 may be a conventional logic circuit inputting either logic 1s or 0s and outputting 0s or 1s. In this embodiment equation 6 must be modified in that previous fine gain control signal fg[p-1] is increased by Δ if b[p] is 1 and previous fine gain control signal fg[p-1] is decreased by Δ if b[p] is equivalent to 0 in fine gain calculation circuit 75.

[0052] Fig. 2b shows a second embodiment of fine logic unit 8. In contrast to the first embodiment shown in Fig. 2a the elements 55 to 75 are replaced by holding circuits 81, 82, 83, 84 and microprocessor 85. Upon processing M samples by distribution circuit 50 and counters 51 to 54, the counter values are stored in holding circuits 81 to 84. Then the counters are reset and are ready for processing the next M samples. Microprocessor 85 then reads out the values of the holding circuits 81 to 84 and calculates a uniformity parameter m_u in compliance with equation (5). Then the microprocessor performs the functionality of holding circuit 71, comparator 72, XOR circuit 73, holding circuit 74 and fine gain calculation circuit 75 as described in connection with Fig. 2a.

[0053] As will be explained later in connection with the simulation result a typical value for M is 120000. As a consequence the required operating frequency of distribution circuit 50 and counters 51 to 54 is substantially higher than the operation frequency of microprocessor 85. Although microprocessor 85 has to perform not only a single operation in order to calculate equation (5) and perform the minimum search a substantial difference in operation speed of roughly a factor 1200 remains for M equivalent to 120000 provided that the processing of the counter values takes 100 microprocessor clock cycles. So even for high-speed applications a general-purpose microprocessor 85 having a moderate clock frequency can be used. The application of standard microprocessors reduces development costs and receiver costs especially for small batch sizes.

[0054] The holding circuits 81 to 84 may be omitted if microprocessor 85 is quick enough to enter all counter values within a short time or a certain number of samples are discarded in an idle period T_i between the blocks of M samples which are counted. In the idle period the microprocessor 85 may read out the counter values.

[0055] In another embodiment the counter values are read out by microprocessor 85 one after another in a distance smaller than MT/I. Then each counter value is reset. In this embodiment the periods of time each counter evaluates are shifted with respect to each other. Since it is assumed that the symbols do not appear in a certain pattern but rather are statistically independent this shift may be acceptable.

[0056] In a third embodiment, which is not shown in a figure, the quantized samples may be directly input into a microprocessor which performs the function of elements 50 to 75 shown in Fig. 2a. Such a circuit structure can be applied only to moderate transfer rates due to operation speed limitation of the microprocessor 85. In this embodiment counters 51 to 54 may be implemented simply by registers which are incremented by an adder logic.

[0057] In a further embodiment subsampling may be performed, i. e. not each sample but rather only e.g. each second or third sample is processed and counted.

[0058] Figure 3 shows a statistic of digitized sample values in the form of a bar graph. The possible digital words 21 are plotted on the x-axis. It is assumed that ADC 6 performs a 3-bit digitization. As a consequence the possible digital words range from 0 to 7. The area 23 of each bar illustrates the number of occurrences of a specific digital word within a sequence of M digital words. Such a statistic could be obtained if one counter is provided for each digital word.

[0059] Figure 4 illustrates counter values for the statistics of Figure 3 for a first subset. The set S of all possible digital words is subdivided into four subsets 22. The first subset S_1 comprises the digital words 0 and 1, the second subset S_2 the digital words 2 and 3, the third subset digital words 4 and 5 and the fourth subset the digital words 6 and 7. The area of the bars having a solid upper boundary represents the counter value of a counter for the respective subset. As a consequence the area of the bar for subset S_1 in Figure 4 should be equivalent to the area of the bars for digital words 0 and 1 in Figure 3. The broken lines 24, more specifically the area of the bars defined by the broken lines, illustrates the constant values k_1, k_2, k_3, k_4 which are subtracted from the counter values in order to obtain difference values. As explained in connection with equation (5) the absolute values of the difference values are added in order to obtain the uniformity parameter m_u. The absolute values of the difference values are represented by the area of the stripes 26 between the solid and the broken lines.

[0060] Figure 5 illustrates the choice of two subsets in a further embodiment of this invention. The set S of possible digital values is subdivided into an outer subset S_1, 41 and an inner subset S_2, 42. The outer subset S_1 comprises the digital words 0, 1, 6 and 7 whereas the inner subset S_2 comprises the digital words 2 to 5. It may be said that the inner subset is chosen in a manner that the difference between any digital word comprised in the inner subset and the average of all digital words is smaller than the absolute difference between any digital word comprised in the outer subset and the average. The average of all digital words in the example explained in connection with Figures 3 to 5 is 4. A uniformity parameter in this embodiment may be calculated by equation (7):

$$m_u = \sum_{a_i \in T_2} \sum_{j=1}^{M} \delta_{a_i}(b_j) - \sum_{a_i \in T_1} \sum_{j=1}^{M} \delta_{a_i}(b_j) - k_1 \qquad (7)$$

[0061] As in Figures 3 and 4, the area of bars 43 and 45 represents the count of digital words within the first subset and the area of bar 44 represents the count of digital words in the second subset. The broken lines 46 represent an offset k_1. The uniformity parameter m_u defined by equation 7 may assume both, positive and negative values. In a preferred embodiment in each adjustment step, the fine gain is changed by a value proportional to the uniformity parameter. Provided that the offset value k_1 is not too big, this is tantamount to saying that the amplification is increased if the count associated with the inner subset is greater than the count of the outer subset.

[0062] The uniformity parameter defined in equation 7 is suitable for being processed by a proportional-integral-differential controller or a fuzzy controller since no minimum search is required.

Simulation

[0063] The performance of the method has been simulated for the case of an optical channel distorted by chromatic dispersion and noise. In this example, a MLSE (Maximum-likelihood sequence estimator) algorithm has been applied for digital equalization, and the parameters utilized in simulation have been selected as:

$M=120'000$
three bit quantization, $n=3$, $2^n=8$
$S_c=\{a_1,a_8\}$
$m_c>M/8$ ($M/8=15'000$)
$S = S_1 \cup S_2 \cup S_3 \cup S_4$, $S_1=\{a_1,a_2\}$, $S_2=\{a_3,a_4\}$, $S_3=\{a_5,a_6\}$ and $S_4=\{a_7,a_8\}$
$k_q=M/4$ ($M/4=30'000$), $1 \leq q \leq 4$

[0064] The simulation results are shown in Fig. 6. In this graph, the coarse gain parameter m_c, the uniformity parameter m_u and the BER are plotted against the normalized signal power. In the low signal power regime e. g. below 0.2 normalized signal power, the digital equalizer 7 produces high BER due to existing unoccupied outer quantization levels. By increasing the signal power, the sequence estimator arrives at the region of the best BER for normalized signal power between 0.6 and 1.2. For the normalized signal power between 0.6 and 1.2 the parameter m_u reaches the minimum value and the parameter m_c is greater than $M/8=15'000$. Further increasing the signal power leads to the quantization overloading that causes an increase of the BER.

[0065] As explained above, the gain of the coarse VGA unit 2 is adjusted first by increasing the coarse gain from lower to higher values. After the m_c exceeds M/8 the coarse gain is kept constant and the fine AGC unit minimizes the uniformity parameter m_u and provides the best signal power indicating the minimum BER.

[0066] For unknown but distorted channel characteristics, the existence of the m_u minimum enables the AGC to deliver useful amplitude statistics for the downstream digital equalizer. Problems of signal-to-noise ratio reduction with undistorted, almost ideal channels are obviated by the coarse AGC and especially by the lower bound on m_c. In this case, the coarse AGC will keep the signal power in some range and the fine AGC will be switched off practically. With an undistorted signal detector, e.g. based on amplitude histogram analysis, or by external configuration command, the fine AGC could really be switched off with the advantage of less dither penalty. Nevertheless, for time-variant channels with distortion the fine AGC demonstrates its performance.

[0067] Further modifications and variations of the present invention will be apparent to those skilled in the art in view of this description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the present invention. It is to be understood that the forms of the invention shown and described herein are to be taken as the presently preferred embodiments.

Claims

1. A method for controlling amplification within a receiver (1) comprising:

   setting the gain of a variable gain amplifier (3) which amplifies an input signal (10) to obtain a gain-controlled signal (12);

   analog-to-digital converting (6) said gain controlled signal (12) thereby generating digital words (15, 20) each digital word having a value of a plurality possible digital values;

   counting digital words having a value within a first subset (S_1) of possible digital values thereby generating a first counter value (51); said counted digital words belonging to a predetermined number of digital words; said first subset (S_1) comprising at least one value;

   characterized by
   counting (52, 53, 54) digital words having a value within a second subset (S_2, S_3, S_4) of possible digital values thereby generating a second counter value;
   said counted digital words belonging to said predetermined number of digital words; said second subset being different from said first subset; said second subset comprising at least one value; and
   setting said gain in accordance with the first and second counter value in a fashion that all counter values are as equal as possible.

2. The method of claim 1, wherein each subset comprises at least two possible digital values.

3. The method of claim 1 or 2, said setting further comprising:

summing all counter values (70) in order to obtain a uniformity parameter; and

setting (8, 18) said gain in order to minimize said uniformity parameter.

4. The method of claim 1 or 2, said setting further comprising:

subtracting a value (24, 55, 56, 57, 58) from each counter value (25, 51, 52, 53, 54) in order to obtain difference values (26); and

summing the absolute values of all said difference values in order to obtain a uniformity parameter; and

setting (8, 18) said gain in order to minimize said uniformity parameter.

5. The method of claim 1, **characterized in that** the absolute difference between any value within said first subset (42) and an average of all possible digital values is greater than the absolute difference between any value within said second subset (41) and said average and
said setting said gain further comprising:

increasing said amplification with the count of said first counter (51) is greater than the count of said second counter (52, 53, 54); and

decreasing said amplification if the count of said first counter is smaller than the count of said second counter.

6. The method of claim 5, said setting said gain further comprising:

calculating the difference of the first counter value minus the second counter value;

adding an offset to said difference in order to obtain a uniformity parameter;

said gain is increased or decreased by a value proportional to said uniformity parameter.

7. A circuit to be used within a receiver comprising:

a variable gain amplifier (3) for receiving an analog signal and outputting a gain controlled signal (12);

an analog-to-digital converter (6) connected to said variable gain amplifier (3) for digitizing said gain controlled signal, thereby generating digital words, each digital word having a value out of a plurality of possible digital values;

a first counter (51) connected to said analog-to-digital converter for counting digital words having a value within a first subset of possible digital values; said counted digital words belonging to a predetermined number of digital words; said first subset (S_1; 41) comprising at least one value;

characterized by:

a second counter (52, 53, 54) connected to said analog-to-digital converter (6) for counting digital words having a value within a second subset (S_2, S_3, S_4; 42) of possible digital values; said counted digital words belonging to said predetermined number of digital words; said second subset (S_2, S_3, S_4; 42) being different from said first subset (S_1; 41); said second subset comprising at least one value; and

a gain calculation circuit (75) for setting said gain in accordance with the values of said first and second counters in a fashion that said values of said counters are as equal as possible.

8. A circuit of claim 7, further comprising an adder (70) which is connected to each of said counters for adding the

counter values; said adder (70) providing its output to said gain calculation circuit (75) which sets said gain in accordance with the output signal of said adder (70).

9. The circuit of claim 7, further comprising:

a first register (55);

a second register (56, 57, 58);

a first absolute difference circuit (59) being connected to said first counter (51) and said first register (55) for calculating the absolute difference between the value of said first counter (51) and the value stored in said first register (55)

a second absolute difference circuit (60, 61, 62) being connected to said second counter (52, 53, 54) and said second register (56, 57, 58) for calculating the absolute difference between the value of said second counter (52, 53, 54) and the value stored in said second register (56, 57, 58); and

an adder (70) connected to each of said absolute difference circuits (59, 60, 61, 62) for adding said absolute differences; said adder (70) providing its output to said gain calculating a circuit (75) which sets said gain in accordance with the output provided by said adder (70).

10. A circuit of claim 7, **characterized in that** the absolute difference between any value within a said first subset (41) and an average of all possible digital values smaller than the absolute difference between any value within said second subset (42) and said average and said circuit further comprising a subtractor for calculating the difference of said first counter value minus said second counter value;
said subtractor providing its output to said gain calculating circuit (75) for setting said gain in accordance with the output of said subtractor.

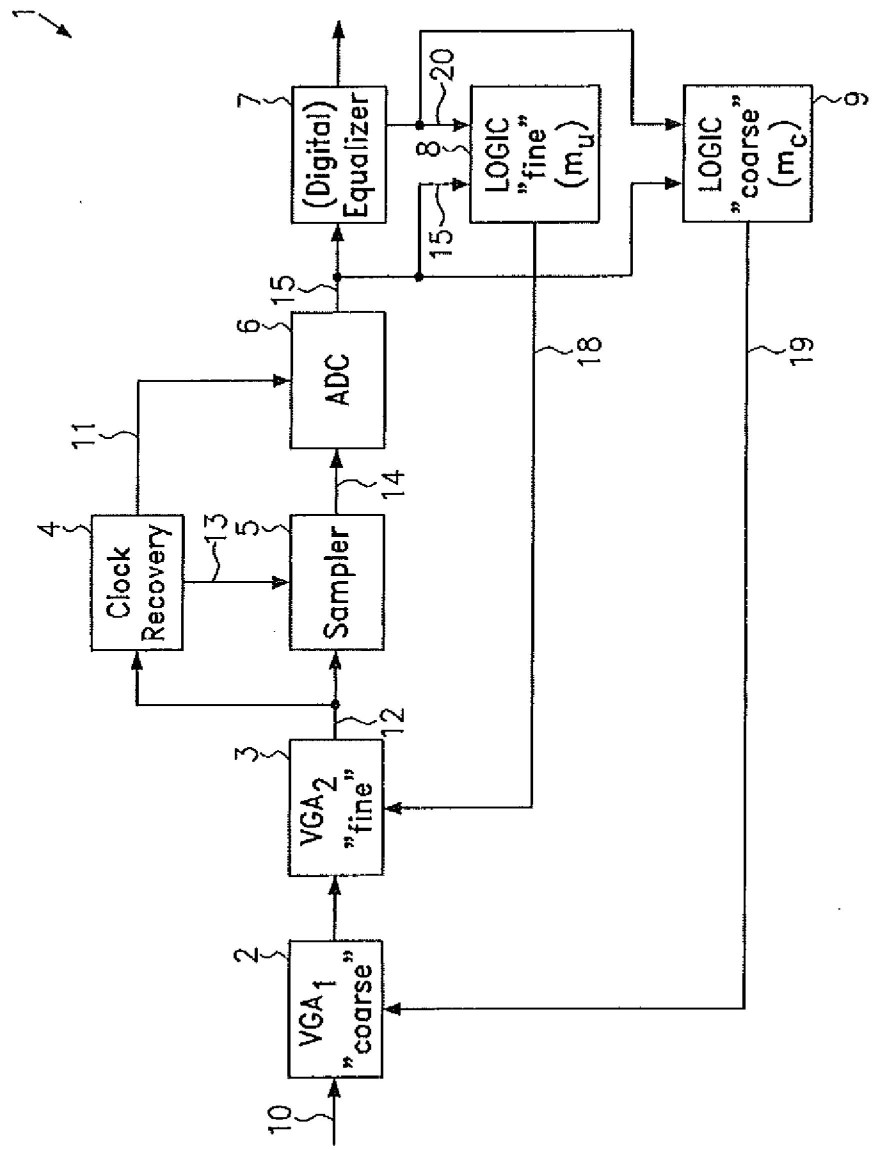
1
VGA1 "coarse"
2
10
VGA2 "fine"
3
12
Clock Recovery
4
13
Sampler
5
14
ADC
6
11
15
(Digital) Equalizer
7
LOGIC "fine" (mu)
8
20
15
18
LOGIC "coarse" (mc)
9
19

Fig.1

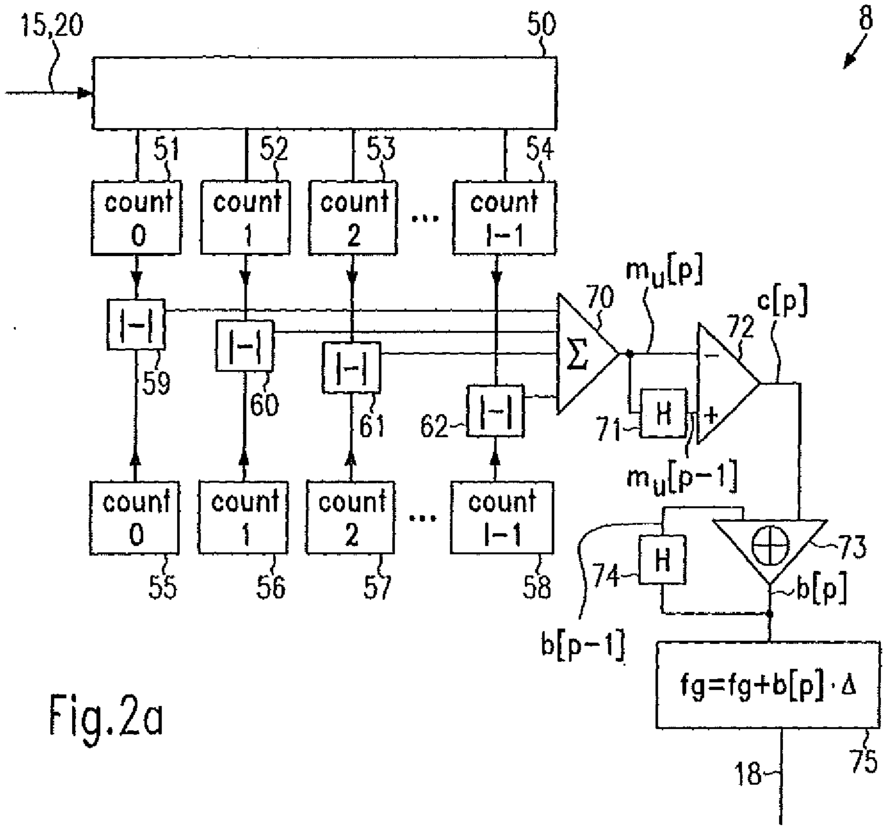
15,20
50
8
51
52
53
54
count 0
count 1
count 2
count I-1
|-|
59
60
61
62
70
Σ
$m_u[p]$
c[p]
72
71
H
$m_u[p-1]$
count 0
count 1
count 2
count I-1
55
56
57
58
73
74
H
b[p]
b[p-1]
fg=fg+b[p]·Δ
75
18

Fig.2a

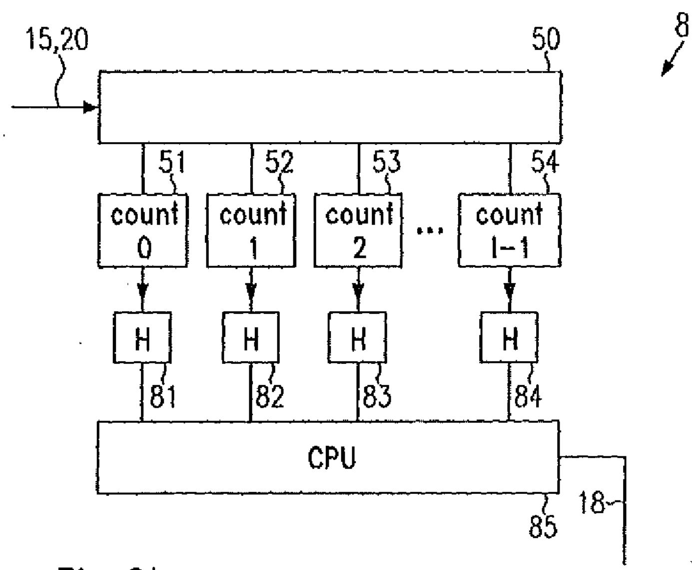
15,20
50
8
51
52
53
54
count 0
count 1
count 2
count I-1
H
81
82
83
84
CPU
85
18

Fig.2b

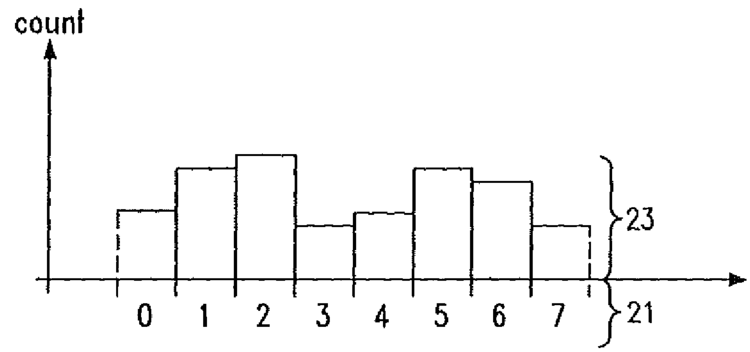

Fig.3

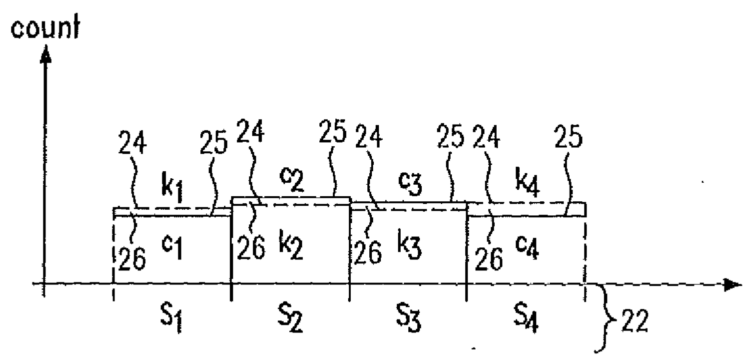

Fig.4

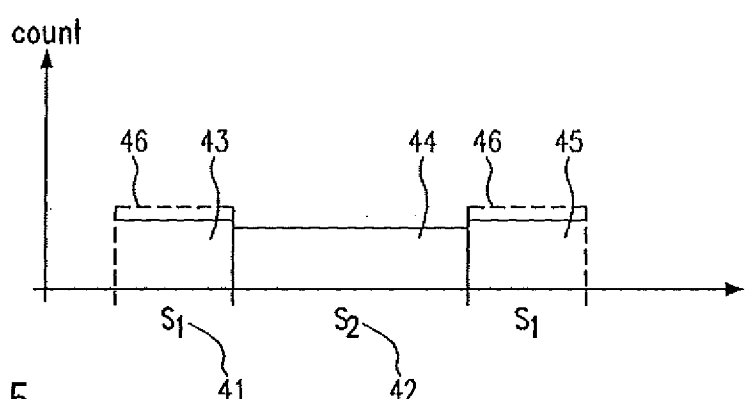

Fig.5

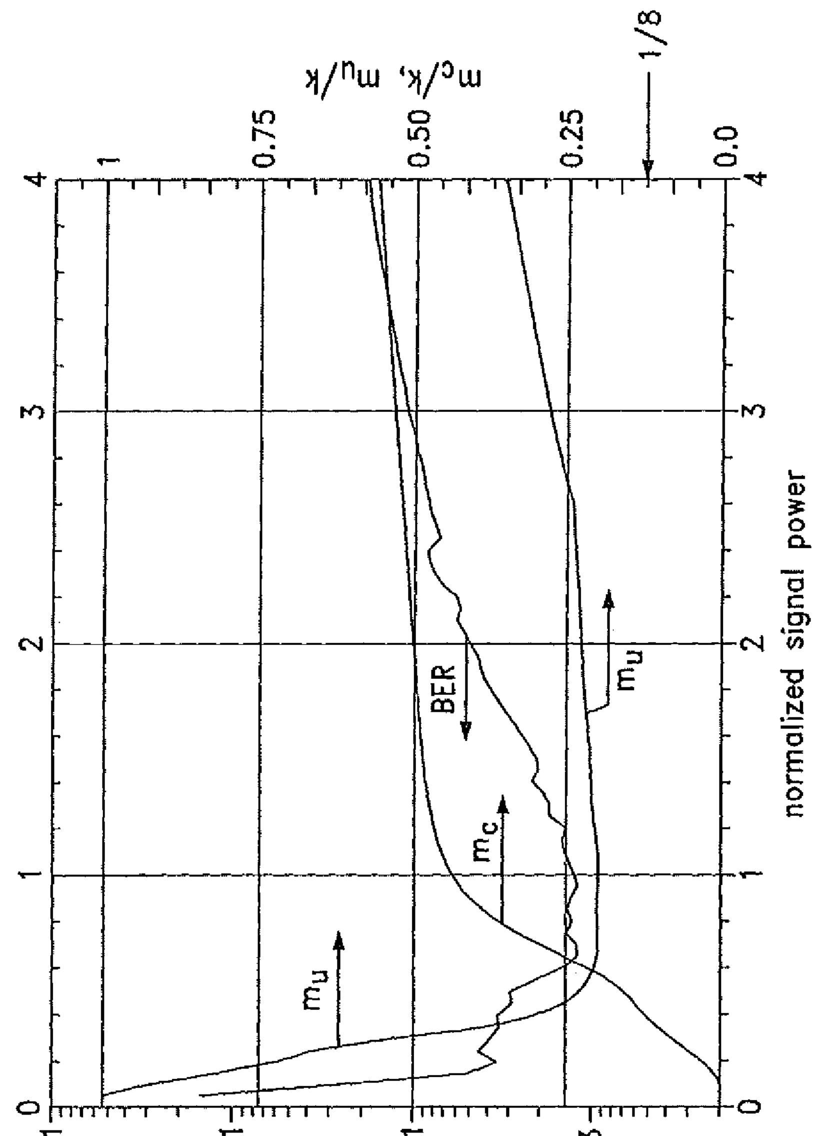
BER
1
0.1
0.01
1E-3
0
1
2
3
4
normalized signal power
m_c/k, m_u/k
1
0.75
0.50
0.25
0.0
1/8
m_u
m_c
BER
m_u

Fig.6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 03 00 9564

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	US 6 038 435 A (ZHANG JIN-YUN) 14 March 2000 (2000-03-14) * abstract * * column 3, line 36 - column 6, line 67; figure 2 * ---	1,7	H03G3/30 H03M1/18
A	US 5 917 372 A (OSAWA TOMOKI ET AL) 29 June 1999 (1999-06-29) * abstract * * column 3, line 52 - column 5, line 61; figures 2,3,5,6 * ---	1,7	
A	US 2002/118779 A1 (WU QIANG ET AL) 29 August 2002 (2002-08-29) * abstract * * page 1, paragraph 16 - page 3, paragraph 28; figure 2 * ---	1,7	
D,A	US 3 931 584 A (MOTLEY DAVID M ET AL) 6 January 1976 (1976-01-06) * abstract * * column 2, line 41 - column 3, line 7 * * column 7, line 59 - column 9, line 15; figure 3 * -----	1,7	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H03G H03M H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	18 September 2003	Trafidlo, R

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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T : theory or principle underlying the invention
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 03 00 9564

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
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18-09-2003

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(71) Applicant: CADENCE DESIGN SYSTEMS, INC. [US/US]; 2655 Seely Avenue, San Jose, CA 95134 (US).

(72) Inventors: BOCCUZZI, Joseph; 77 Robin Court, Staten Island, NY 10309 (US). HWANG, Syang-Myau; 295 Santa Ana Court, Sunnyvale, CA 94086 (US). RAO, Roopa; 420 Riverside Court, Apt. 206, Santa Clara, CA 95054 (US).

(74) Agent: CARPENTER, John, W.; Crosby, Heafey, Roach & May, Two Embarcadero Center, Suite 2000, San Francisco, CA 94111 (US).

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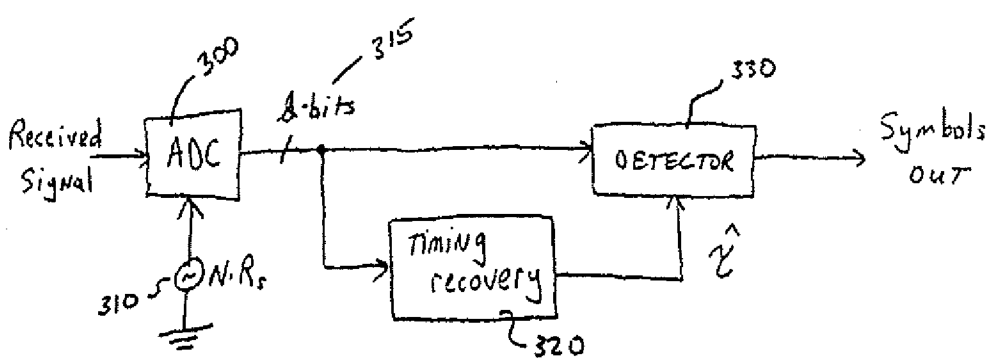
(54) Title: SYMBOL TIMING RECOVERY METHOD FOR LOW RESOLUTION MULTIPLE AMPLITUDE SIGNALS



(57) Abstract: Symbol timing is performed by providing a histogram of samples of a signal for a predetermined number of symbol times. An average, weighted average, or other method is applied to determine an average timing for a max eye opening for each symbol time. The average max eye opening timing is applied to an edge detection of a currently received signal to determine timing of a sample that is most likely to occur closest to the max eye opening for the current symbol. The invention may also be practiced based on a center timing of each symbol.

WO 02/30035 A1

SYMBOL TIMING RECOVERY METHOD FOR LOW RESOLUTION MULTIPLE AMPLITUDE SIGNALS

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BACKGROUND OF THE INVENTION

Field of Invention

This invention relates to recovery of symbol timing of a signal received in a digital communication system. The invention is more particularly related to the detection of symbol edges for use in symbol timing recovery of low resolution digital signals encoded in an analog received signal.

Discussion of Background

In general digital communication systems, a transmitting apparatus modulates a digital signal (1) by any known modulation techniques (Quadrature Amplitude Modulation (QAM), or Quadrature Phase Shift Keying (QPSK), for example). The modulation technique converts the digital signal into an analog signal for transmission. A receiver of the analog modulated signal demodulates the signal and converts it into a digital signal, restoring it to the original form (digital signal (1)).

Many modulation and demodulation techniques are know that are capable of accurately restoring the received signals into original digital signals (also referred to as symbol values) when the received signals are sampled at the same interval of time (frequency) and symbol starting point (phase) as those of the symbols transmitted from the transmitter. Without proper frequency and phase alignment in the receiver (Rx), increased computations are required to maintain accuracy of the digital signal restoration, or additional errors are encountered (increasing a bit error rate (BER) of the communications system in general, and the receiver in particular). Therefore, one of the important processes that occur in the receiver of the digital communication system is to accurately

restore a symbol timing (frequency and phase) representing a point in time that the received signal should be sampled.

In some systems, a specific carrier corresponding to a sampling frequency is transmitted, providing frequency and phase for the sampling. However, many modern systems do not provide a carrier, and it is therefore important to accurately recover a symbol timing using only the received signal. With the proliferation of digital communication systems, there has been an increased need for improved and distinctive symbol timing recover (STR) processes within receivers of digital communications. A conventional apparatus for recovering a symbol timing is shown in FIG. 1.

In FIG. 1, a received signal is input to an analog-to-digital (A/D) converter 100. The A/D converter 100 samples the input signal at a frequency supplied from a voltage controlled oscillator (VCO) 110 and converts the analog signal into a digital signal. The digitized signal is output via a matching filter 120, and simultaneously input to a timing error detector 130. The timing error detector 130 detects a symbol timing error from the input signal and outputs a detected error value, to a loop filter 140. The loop filter 140 filters the input signal to remove various noises. The VCO 110 oscillates at a frequency according to the output of the loop filter 140 and supplies the oscillated frequency signal to the A/D converter 100.

However, in conventional systems, receiver (Rx) and transmitter (Tx) inaccuracies, operating conditions, and other reasons can cause symbol timing drift that results in the number of symbols transmitted from the transmitter differs or has significantly different timing from that of the restored signals. For example, one reason is because the receiver does not know when the symbols will arrive, which can be due to a number of factors, including propagation delay between the Tx and Rx, particularly in a wireless communication environment where distances may become large. Another reason is that the transmitter and receiver clocks drift from their nominal values, forcing the receiver to continually adjust (or adapt) to maintain the appropriate sample time instance. By appropriate, it is desired that the sampling time instance match (or closely match) a maximum eye opening of the received signal, since this timing epoch corresponds to a maximum signal to noise ratio (SNR) value of the received signal.

One common method for continually adjusting to maintain the appropriate sample time instance is known as matched filter technique, which is illustrated in Fig. 2. In Fig. 2, a fixed oscillator 200 generates a constant frequency signal and supplies the same to an A/D converter 210. The A/D converter 210 converts the received signal into a digital signal using the frequency signal supplied from the fixed oscillator 200, and outputs the digitized signal to an interpolator 220. Meanwhile, a controller 230 receives a symbol timing error signal output from a timing error

detector 250 via a loop filter 240. The controller 230 generates an interpolation coefficient according to the input symbol timing error signal and supplies the same to the interpolator 220. The interpolator 220 interpolates the digitized signal with the interpolation coefficient supplied from the controller 230, and outputs the interpolated result to a matching filter 260.

The A/D converter 210 samples the received signal at a sampling frequency supplied from the fixed oscillator 200 and converts the analog signal to the digital signal. The digitized signal is output via the interpolator 220 and the matching filter 260 and simultaneously input to the timing error detector 250. The symbol timing error signal which is detected in the timing error detector 250 and has noise removed in the loop filter 240 is then input to the controller 230. The controller 230 generates the interpolation coefficient according to the input signal. The interpolator 220 interpolates the digitized signal according to the interpolation coefficient supplied from the controller 230, and thereby removes the symbol timing error. Although this apparatus can accurately recover the symbol timing, it is very complicated to implement using hardware.

However, none of these techniques provide the best solution for modern digital communications devices. Moreover, the above techniques favor high resolution received signals. In this application, resolution refers to discrete time representations of a continuous signal. High resolution refers to a relatively large amount of bits in the ADC. For example, a number of bits (b), such as b >= 6, are considered high resolution.

SUMMARY OF THE INVENTION

The present inventors have realized that modern digital communications systems fail to address the needs of applications of low resolution digital systems.

The present invention provides a robust method with good BER performance for low resolution signals. The present invention can be implemented without the complexities seen in the prior art, and can be modified for improved performance when high resolution signals are available.

Roughly described, the present invention provides Symbol Timing Recovery (STR) via a set of edge detections maintained in a histogram that are utilized to calculate the phase and timing of subsequently received symbols.

The present invention is embodied as a device, comprising, an ADC mechanism configured to sample a received signal at a predetermined over-sampling rate, a detector connected to said ADC mechanism and configured to detect a symbol identified by at least one of said samples during predetermined symbol times, and a symbol timing mechanism connected to said ADC mechanism and said detector and configured to read said samples and adjust a timing of the detection performed

by said detector based on previously read samples so that the detected samples are at a most likely maximum eye opening of said samples during said predetermined symbol times.

The present invention includes a method of symbol timing, or recovery of symbol timing, comprising the steps of, sampling a received signal at a predetermined over-sampling rate, determining a timing for detection of a specific one or set of said samples based on historical data of samples previous samples, and detecting said specific one or predetermined number of samples based on the determined timing.

Both the device and method may be conveniently implemented on a general purpose computer, or networked computers, and the results may be displayed on an output device connected to any of the general purpose, networked computers, or transmitted to a remote device for output or display.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

Fig. 1 is conventional apparatus for recovering a symbol timing;

Fig. 2 is a block diagram illustrating a conventional matched filter technique for continually adjusting to maintain an appropriate sample time instance;

Fig. 3 is a block diagram illustrating the Symbol Timing Recover section in a digital receiver;

Fig. 4A is a graph illustrating a waveform of a digitally sampled continuous analog signal;

Fig. 4B is a graph illustrating a waveform of a digitally sampled low resolution continuous analog signal;

Fig. 5 is a flow chart illustrating a detector adjustment process according to the present invention;

Fig. 6 is a block diagram of a symbol edge detection device according to one embodiment of the present invention;

Fig. 7 is a flow chart illustrating one embodiment of a process for utilizing histogram data for determining a most likely eye opening for a next symbol time;

Fig. 8 is a flow chart illustrating one embodiment of maintaining a running average of timing for a most likely max eye opening of a next symbol time;

Fig. 9 is a block diagram of a symbol center value detection device according to another embodiment of the present invention;

Fig. 10 is an example timing chart of symbol and e value determinations according to the present invention;

Fig. 11A is a set of histogram plots for varying numbers of symbols (M) developed for an Rx eye diagram;

Fig. 11B is a 4 level eye diagram, prior to ADC, using a flex-paging protocol for demonstration purposes;

Fig. 12 is a set of receiver Eye diagrams and corresponding histograms for analyzing performance of a rising edge embodiment of the present invention with a low SNR signal;

Fig. 13 is a set of receiver Eye diagrams and corresponding histograms for analyzing performance of a center detection embodiment of the present invention with a low SNR signal;

Fig. 14 is a set of graphs illustrating BER vs. Eb/No (dB) performance of various embodiments of the present invention vs. ideal and theory STR's;

Fig. 15 is a set of graphs illustrating BER vs. Eb/No (dB) performance of various embodiments of the present invention vs. ideal and theory STR's, including 2-FM (binary frequency shift keying) and 4-FM (4 level frequency shift keying) theory.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In a digital communications system, a number of bits used in the Analog to Digital Converter (ADC) comprises a tradeoff between power consumption, board real estate, and performance. In the present invention, low resolution signals are targeted (for example, signals used in pagers). An example low-resolution system would, for example, choose b = 2 bits for the ADC and 4-level baseband signals (low frequency content signals with discrete amplitude levels and carrier removed, for example).

Referring again to the drawings, wherein like reference numerals designate identical or corresponding parts, and more particularly to Fig. 3 thereof, there is illustrated a block diagram illustrating the Symbol Timing Recover section in a digital receiver. A received signal is fed to an ADC 300 which is timed via an oscillator 310. The digitally converted signals b-bits 315 are fed to a timing recovery module 320 and a detector 330. The timing recovery module 320 identifies the symbol edge and adjusts the phase of detector 330 such that the detector 330 recognizes the symbol at an amplitude sufficient to recover a bit value previously represented in the received signal. The recovered bits, or symbols, are output.

Fig. 4A is a graph illustrating a waveform of a digitally sampled continuous analog signal (for 8x over-sampling). In this example, over-sampling is the number of digital bits converted from

the received signal for a length of time equivalent to a period of a single bit in the digital waveform to be recovered. Thus, fig. 4A shows 8 samples, at times y_0, y_1, y_2, y_3, y_4, y_5, y_6, and y_7, each provided by the ADC, from which a symbol is to be recovered. For the eye diagram of fig. 4A, the detector would want to detect the symbol at $t = y_3$ because y_3 represents the time at which the eye is at maximum (greatest amplitude of the symbol to be recovered).

When using a matched filter approach, each digitally sampled waveform (Fig. 4A, or 4B, for example) is compared to a stored waveform that represents (or "looks" like) a waveform that is expected to be received. Each sampled waveform is compared, and a stored waveform having the highest correlation to the sampled waveform is chosen for output.

Fig. 4B is a graph illustrating a waveform of a digitally sampled low resolution continuous analog signal (for 8x over-sampling). The digitally sampled signal shows a flattening effect 420. The lost information (additional amplitude at the sample points missing due to low resolution) makes matching more difficult because less variance between signals makes each signal have less correlation to the stored waveforms.

Therefore, it can be seen that the matched filter technique works well with high resolution signals. However, with low resolution signals, performance is degraded because much of the information contained in the signal is lost due to resolution reduction.

The present invention observes symbol (or bit) edges in the received digitally sampled signal, and develops a histogram (normalized histogram, or probability density function, normalized by the total number of events, for example) of the boundaries of each symbol. Fig. 5 is a flow diagram that shows the basic process. At step 500, a sample is taken (MSB, for example). At step 510 a second MSB sample is taken. The samples (MSB's in this example) are compared to determine if a transition has occurred (step 520). A transition is detected by determining if Sample 1 (S1) and Sample 2 (S2) are different (different samples indicates a transition, equivalent, or roughly equivalent samples indicate no transition).

The detection information is used to develop a histogram that identifies timing and recovery of past edges or transitions of the sampled received signal. With each transition, the histogram is updated (step 530). The histogram is utilized to adjust the detector (step 540). The detector can be adjusted to any of edge, center, or other portions (1/4, for example) of the incoming symbols, depending on the type of detector used. To finish the loop, S1 is substituted with S1 and the loop continues (step 550). Variations of the flow illustrated in Fig. 5 can be made based on the present disclosure.

Fig. 6 illustrates a block diagram of a symbol edge detection device according to one embodiment of the present invention. In Fig. 6, ADC 600 provides an MSB and a LSB recovered by sampling of a received signal ($b = 2$).

An edge detector 610 compares adjacent MSB samples. The edge detector 610, in this example, is constructed from a delay circuit 612 and an exclusive or circuit device 614. Alternatively, the edge detector may be constructed from other configurations of parts, including, for example, a delay circuit and a comparator. What is important is that the edge detector is capable of determining a transition of the MSB (or other sampled bit). The edge detected (e) is then fed to an N-bin histogram 620. In one embodiment, the n-bin histogram 620 is constructed of a memory device that maintains a history of timing for each edge detected. In another embodiment, one or more averages of edge detectors are calculated and stored.

A detector 640 detects a bit in the sampled received signal at a point that is most likely to be the highest amplitude of the bit being recovered from the received signal. A center adjust device 630 utilizes the histogram 620 to determine the point where the highest amplitude occurs based on previous edge detections. For example, if the last n edge detections each came in at a same time instance interval, that same interval would be the most likely next edge and the most likely point of highest amplitude would be calculated based on that interval. Using specific values, if each symbol is received in .25 ms intervals, the next highest amplitude point could be calculated at .25ms + Ts/2, where Ts = the timing period of the received bits.

In other words, the edge detector compares adjacent MSB samples. If the adjacent samples are the same, then $e = 0$; which indicates that a transition has not occurred. If the adjacent samples are different, then $e=1$; indicating that an edge has been detected. When an edge is found, the time instances (time samples from where the edge was found) are distributed into the N-bin histogram 620. In one embodiment, $N=8$ represents the over-sampling ratio of the ADC (the number of samples per bit or symbol).

Thus, statistics for an edge detection are gathered. The statistics are accumulated for a pre-determined number of Symbols M ($M = 40$, for example). Using the accumulated statistics, a most likely (ML) position of a symbol edge can be determined. For example, given a set of accumulated statistics, and assuming an eye that is at least somewhat symmetrical, the center adjustment is made such that eye is assumed to be at a detected edge, plus Ts/2, Ts being the symbol time (period of the symbols being decoded). Ts is calculated based on the histogram data. Ts is calculated using any method, peak-to-peak, for example. Ts, generally being constant, is known ahead of time. However, it is not known where in the histogram the peaks or Ts will fall. In addition, other factors affect

timing and placement of Ts, such as propagation time delay, frequency drift of transmitter/receiver, interference, etc. Ts may equal T, or be some multiple or fraction thereof (.9T, 1.1T, for example).

The histogram may be constructed and maintained in many different ways. What is important is that a timing of a most likely max eye opening either be maintained or be derivable from data stored in the histogram. For example, Fig. 7 provides a flow chart of one embodiment of a process for using histogram data storing the timing of a max eye opening for each set of samples for each symbol time. At step 700, the samples from a sample period are read. The read samples are compared to determine the max eye opening (highest amplitude, for example) (step 710). A timing of the max eye opening from an edge detection of the symbol time to the max eye opining is stored in the histogram (step 720) (max eye opening). If all the stored samples are not yet read, samples from another period (symbol time) are read and the process repeats (step 740). If all the stored samples are read, an average or other method is utilized to determine a most likely max eye opening for a next symbol time (step 750). The most likely max eye opening for the next symbol time is then added to the timing of an edge detection of the next symbol time to provide a timing for the detector to detect the symbol value.

Other histogram configurations and processes may be utilized to determine the detection timing. Fig. 8 illustrates another embodiment where a running average of max eye opening timing relative to edge detection is maintained. At step 800 sample data is collected for a symbol time of a received signal. The collected sample data is analyzed to determine a timing of the max eye opening of the collected sample data symbol time (step 810). A running average or other statistic representing a most likely max eye opening for a next symbol time is then adjusted based on the max eye opening timing of the collected sample data (step 820). The running average is then applied to the edge detection of the next symbol time to provide a detection timing for the symbol.

Fig. 9 illustrates a block diagram of another embodiment of the present invention. In this embodiment, a symbol center value is determined. ADC 600 provides an MSB and a LSB recovered by sampling of a received signal (b = 2). A transition detector 910 compares adjacent MSB samples. The transition detector 910, in this embodiment, is constructed from a delay circuit 912 and an exclusive or circuit device 914. Alternatively, the transition detector may be constructed from other configurations of parts, including, for example, a delay circuit and a comparator. What is important is that the edge detector is capable of determining a transition of the MSB (or other sampled bit) (an edge triggered device, for example, outputting a fixed value when the input goes from zero to high, and outputting zero when the input falls).

The value output from the transition detector 910 is e, pulse synched with the symbol boundaries. An illustration is provided by Fig. 10. An MSB is illustrated cycling high for a time period t_1, low for a time period t_2, and back high for time period t_3. e is shown pulsing high at each transition (1000, 1005, 1010, and 1015).

The edge detected (e) is then inverted by inverter 915. The inverted edge (e bar 1020) is a signal that pulses high at each symbol center. The e bar 1020 signal is fed to a rising edge true device 925. The rising edge true device, which operates as a dirac delta type function (impulse type function), or one cycle of a fast (fastest) clock cycle, for example, to produce e_R 1030. The verified rising edge value e_R is fed to an N-bin histogram 920, where it is saved. In this embodiment, the center value is adjusted directly, rather than using the edge detection plus ½ a symbol time.

Fig. 11A is a set of histogram plots for varying numbers of symbols (M) developed for a received signal (see Rx eye diagram). The SNR for the illustrated diagrams is 10 dB. The histogram plots provide an analysis of performance of various embodiments of the present invention. Histogram for each of M = 10, 20, 40, and 80 are shown. As can be seen from the diagrams, in general, the edge detections are consistent and provide a reasonable estimate of symbol time. However, the eye diagrams show corresponding better averages with increasing numbers of histograms averaged (note more distinct peaks, at symbol times 1 and 2, for example, and the flattening of non symbol time areas, at approximately .25 and .75, for example, as the number of symbols increases).

Fig. 11B is a 4 level eye diagram, prior to ADC, using a flex-paging protocol for demonstration purposes. The present inventors obtained good results using a receiver bandpass filter having 8kHz bandwidth, and a post detection filter having a 2 kHz bandwidth.

Fig. 12 is a receiver Eye diagram and corresponding histogram for analyzing performance of a rising edge embodiment of the present invention with edge detection and a low SNR signal. The Rx eye chart shows the received signal, and the M=80 histogram illustrates consistent, symmetrical, symbol times.

Fig. 13 is a receiver Eye diagram and corresponding histogram for analyzing performance of a center detection embodiment of the present invention with a low SNR signal. Again, the Rx eye chart shows the received signal, and the histogram illustrates consistent, symmetrical, symbol times.

In most cases, system performance is equivalent whether using an edge or center detection embodiment. However, the system has more jitter in it, then the edge detector histogram will be less peaky, more flat. In this case, a system designer would want to go with FIG. 13, center detection, because jitter means there is uncertainty. If you don't have any jitter, then the designer would want

to go with the edge detector. In one embodiment, both center and edge detection is provided, giving the option of choosing one versus the other, depending on what the overall received signal is.

Fig. 14 is a set of graphs illustrating BER vs. Eb/No (dB) performance of various embodiments of the present invention vs. ideal and theory STR's. As can be seen in the graph, BER performance for each of N=20, 40, 80, and 160 are grouped in close proximity of an ideal STR. The ideal STR is seen grouped with the N= 200..160 group, and deviated from a Theory STR by approximately 1 dB at each portion of the graph. In an implementation of the invention, the number of histograms considered can be varied depending on any factor (dB required, or available processing power, for example). When additional processing power is available or additional dB needed, M may be set to a higher value (160, for example), but in low dB situations (pilot signal, for example), a lower value such as 20 may be sufficient.

Fig. 15 is a set of graphs illustrating BER vs. Eb/No (dB) performance of various embodiments of the present invention vs. ideal and theory STR's, including 2-FM and 4-FM theory.

Portions of the present invention may be conveniently implemented using a conventional general purpose or a specialized digital computer or microprocessor programmed according to the teachings of the present disclosure, as will be apparent to those skilled in the computer art.

Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will be apparent to those skilled in the software art. The invention may also be implemented by the preparation of application specific integrated circuits or by interconnecting an appropriate network of conventional component circuits, as will be readily apparent to those skilled in the art.

The present invention includes a computer program product which is a storage medium (media) having instructions stored thereon/in which can be used to control, or cause, a computer to perform any of the processes of the present invention. The storage medium can include, but is not limited to, any type of disk including floppy disks, mini disks (MD's), optical discs, DVD, CD-ROMs, micro-drive, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, DRAMs, VRAMs, flash memory devices (including flash cards), magnetic or optical cards, nanosystems (including molecular memory ICs), RAID devices, remote data storage/archive/warehousing, or any type of media or device suitable for storing instructions and/or data.

Stored on any one of the computer readable medium (media), the present invention includes software for controlling both the hardware of the general purpose/specialized computer or microprocessor, and for enabling the computer or microprocessor to interact with a human user or other mechanism utilizing the results of the present invention. Such software may include, but is not

limited to, device drivers, operating systems, and user applications. Ultimately, such computer readable media further includes software for performing the present invention, as described above.

Included in the programming (software) of the general/specialized computer or microprocessor are software modules for implementing the teachings of the present invention, including, but not limited to, comparing consecutive MSB values, maintaining a histogram of signal samples, averaging max eye openings of sample sets, adjusting detection times, and the display, storage, or communication of results according to the processes of the present invention.

Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

WHAT IS CLAIMED IS:

1. A symbol timing device, comprising:

an ADC mechanism configured to sample a received signal at a predetermined over-sampling rate;

a detector connected to said ADC mechanism and configured to detect a symbol identified by at least one of said samples during predetermined symbol times; and

a symbol timing mechanism connected to said ADC mechanism and said detector and configured to read said samples and adjust a timing of the detection performed by said detector based on previously read samples so that the detected samples are at a most likely maximum eye opening of said samples during said predetermined symbol times.

2. The symbol timing device according to Claim 1, wherein :

said symbol timing mechanism comprises,

a histogram device configured to,

store a histogram of said samples over a predetermined number of said symbol times, and

calculate a most likely max eye opening of said samples of a next symbol time based on said histogram, and

an adjustment device configured to adjust said timing of the detection performed by said detector based on the calculated most likely max eye opening.

3. The symbol timing device according to Claim 2, wherein:

said over-sampling rate is N; and

said histogram device comprises,

a memory configured to store M sets of samples, each sample set comprising N samples, and each sample set corresponding to one of said predetermined symbol times, and

a calculation mechanism configured to determine said most likely eye-opening of said set of samples of a next symbol time based on the sample sets stored in said histogram.

4. The symbol timing device according to Claim 2, wherein said histogram device comprises a calculator configured to calculate said most likely max eye opening by averaging max eye openings of said samples over said predetermined number of symbol times.

5. The symbol timing device according to Claim 1, wherein :

said symbol timing mechanism comprises,

an edge detector configured to determine an edge of symbols sampled by said ADC mechanism;

a histogram configured to save samples from said ADC for a predetermined number of previous symbol times; and

a center adjustment mechanism configured to adjust a sample detected by said detector based on said histogram and edges detected by said edge detector.

6. The symbol timing device according to Claim 5, wherein :

said edge detector comprises,

a delay mechanism having an input connected to said ADC mechanism, and an output, and

an exclusive or device having one input connected to said ADC mechanism, a second input connected to the output of said delay mechanism, and an output connected to said histogram; and

said histogram uses the output of said exclusive or to identify samples maintained in said histogram.

7. The symbol timing device according to Claim 1, wherein :

said symbol timing mechanism comprises,

a transition detector configured to determine an edge of symbols sampled by said ADC mechanism and output a transition detected signal,

a conversion mechanism configured to convert the transition detected signal to a pulse synched with a center of symbols corresponding to detected transitions, and

a histogram that maintains data on a predetermined number M of said pulses;

said detector is further configured to detect symbols based on the data maintained in said histogram.

8. The symbol timing device according to Claim 7, wherein said center adjustment mechanism is further configured to adjust time that said symbol is detected by said detector.is based on an average of past pulses.

9. The symbol timing device according to Claim 7, wherein said center adjustment mechanism is further configured to adjust time that said symbol is detected by said detector is based on a weighted average of past pulses.

10. The symbol timing device according to Claim 7, wherein :

said conversion mechanism comprises,

an inverter connected to said transition detector and configured to invert the transition detect signal such that the inverted signal is now synched with a center of a symbol that caused the transition detection and

a rising edge detect mechanism connected to said inverter and configured to convert the synched signal to a pulse by said rising edge detect mechanism.

11. A method of symbol timing recovery, comprising the steps of:

sampling a received signal at a predetermined over-sampling rate;

determining a timing for detection of a specific one or set of said samples based on historical data of samples previous samples; and

detecting said specific one or predetermined number of samples based on the determined timing.

12. The method according to Claim 11, further comprising the step of:

adjusting said timing based on newly acquired samples.

13. The method according to Claim 11, further comprising the step of:

maintaining a histogram of sample sets, each set comprising a predetermined number of samples for each of a predetermined number of symbol times;

wherein said step of determining a timing comprises the steps of,

averaging a max eye opening of each set of samples maintained in said histogram, and

calculating a most likely max eye opening for a next set of samples based on the average max eye opening.

14. The method according to Claim 13, wherein said step of averaging comprises performing a weighted average of said max eye openings of each set of samples maintained in said histogram.

15. The method according to Claim 11, further comprising the step of:

maintaining a histogram comprising a running average of timing of a max eye opening of samples for each of a predetermined number of symbol times;

wherein said step of determining a timing for detection of a symbol comprises using the running average.

16. The method according to Claim 11, further comprising the steps of:

maintaining a histogram indicating timings from an edge detection to max eye opening of the sampled signal during past symbol times;

averaging the timings of past symbol time max eye openings; and

detecting an edge of a symbol contained in the current sampled signal;

wherein said step of determining a timing comprises, applying the averaged past symbol max eye opening timing to a timing of the detected symbol edge of the current sampled signal.

17. The method according to Claim 16, wherein said step of detecting an edge comprises the steps of:

delaying the received signal by one symbol time;

comparing a currently received signal and the delayed signal; and

signaling an edge detection if the compared signals are at different logic levels.

18. The method according to Claim 16, further comprising the steps of:

inverting the detected edge so that the rising edge of the inverted signal corresponds to a center of a symbol time of the symbol for which the edge was detected;

converting the inverted signal into a pulse; and

wherein:

said step of determining a timing comprises applying each pulse as a timing for detecting said specific one or set of said samples.

19. The method according to Claim 18, further comprising the step of:

adjusting a timing of said pulse based on data contained in said histogram.

20. A symbol timing device, comprising:

ADC means for sampling a received signal at a predetermined over-sampling rate;

detector means for detecting a symbol identified by at least one of said samples during a predetermined symbol time; and

symbol timing means for reading said samples and adjust a timing of the detection performed by said detector based on previously read samples so that the detected samples are at a most likely maximum eye opening of said samples.

21. The symbol timing device according to Claim 20, wherein :

said symbol timing means comprises,

histogram means for storing a histogram of said samples and determine a most likely max eye opening of said samples based on said histogram, and

adjustment means for adjusting said timing of the detection performed by said detector based on said histogram determined most likely max eye opening.

FIG. 1 (PRIOR ART)

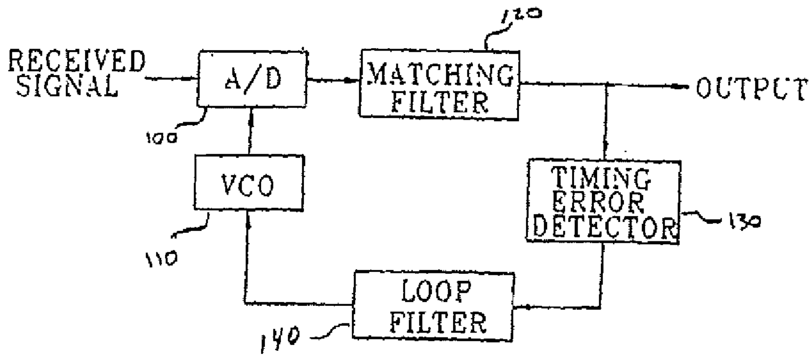
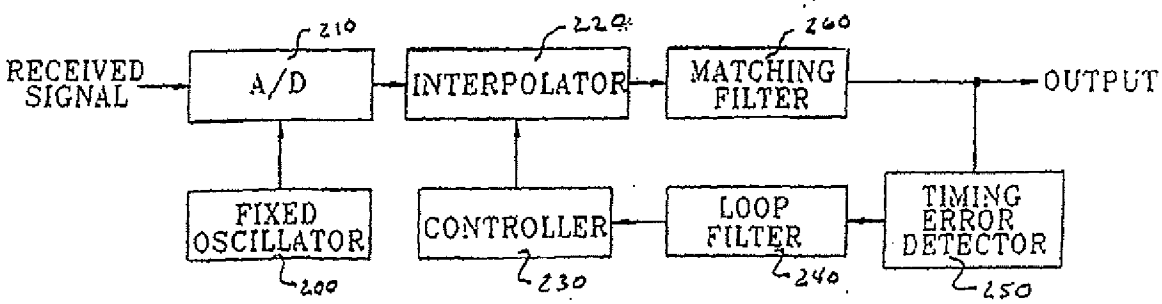


FIG. 2 (PRIOR ART)



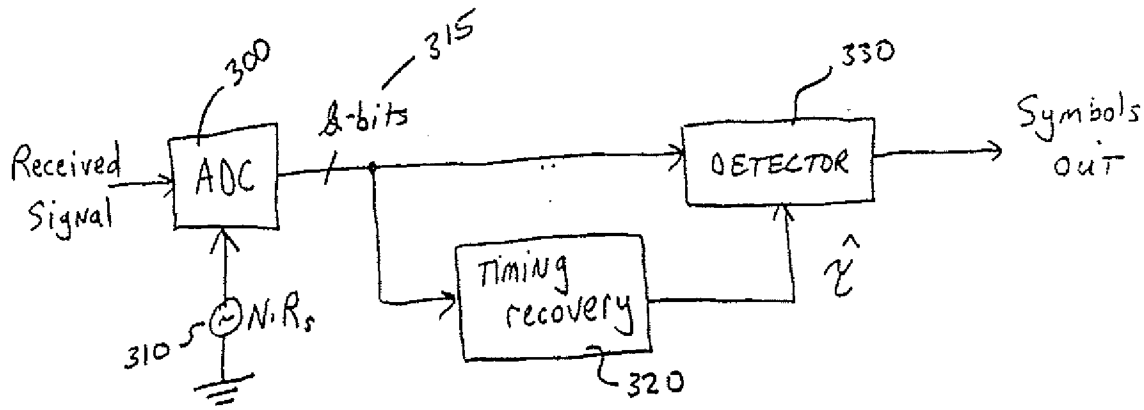

300
315
330
Received Signal
ADC
b-bits
DETECTOR
Symbols out
Timing recovery
$\hat{\tau}$
310
$N \cdot R_s$
320

FIG. 3

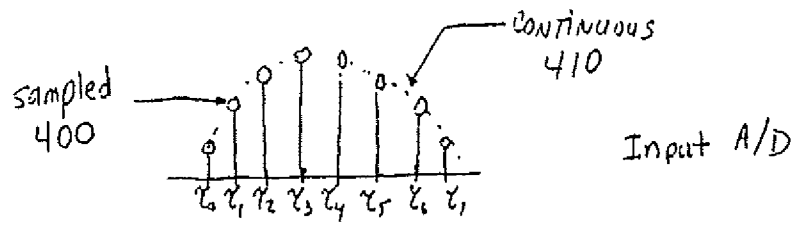

continuous
410
sampled
400
Input A/D
τ_0 τ_1 τ_2 τ_3 τ_4 τ_5 τ_6 τ_7

FIG. 4A

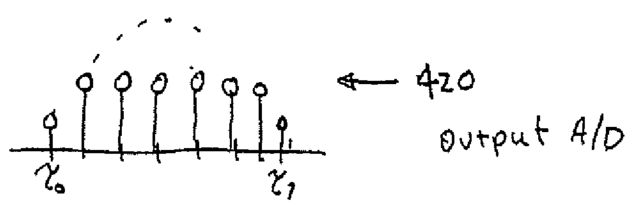

420
output A/D
τ_0
τ_7

FIG. 4B

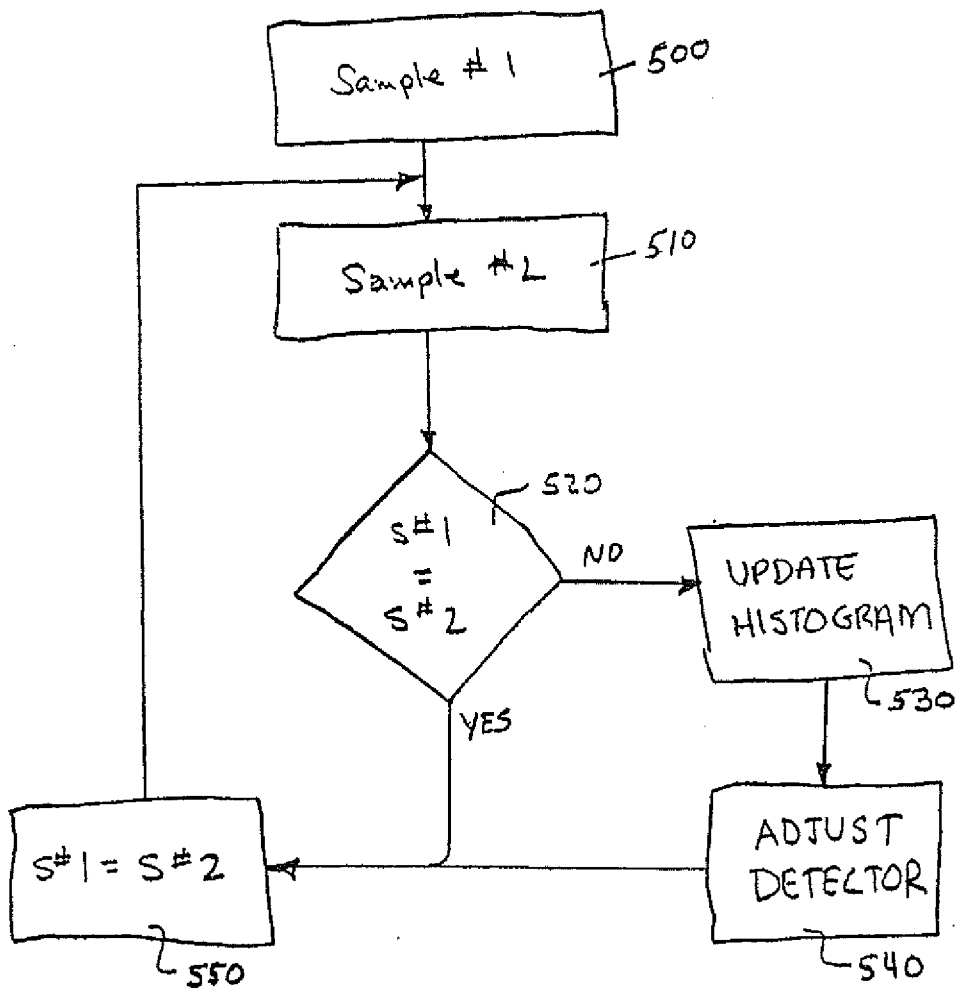

Sample #1
500
Sample #2
510
S#1 = S#2
520
NO
UPDATE HISTOGRAM
530
YES
ADJUST DETECTOR
540
S#1 = S#2
550

FIG. 5

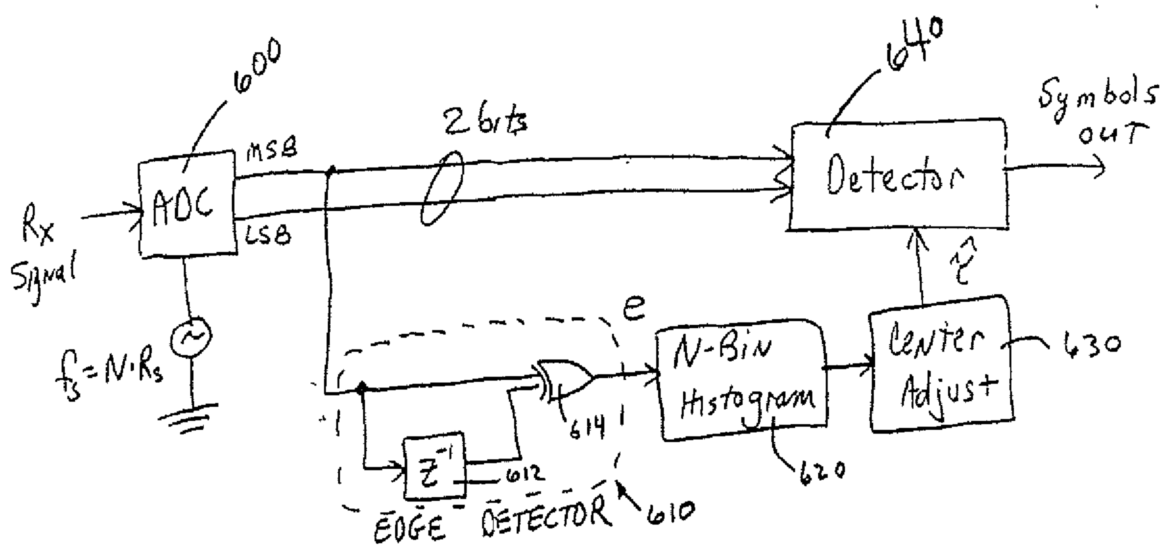

600
640
Symbols out
2 bits
MSB
LSB
ADC
Detector
Rx Signal
$f_s = N \cdot R_s$
e
N-Bin Histogram
Center Adjust
630
$\hat{\tau}$
z^{-1}
612
614
620
EDGE DETECTOR
610

FIG. 6

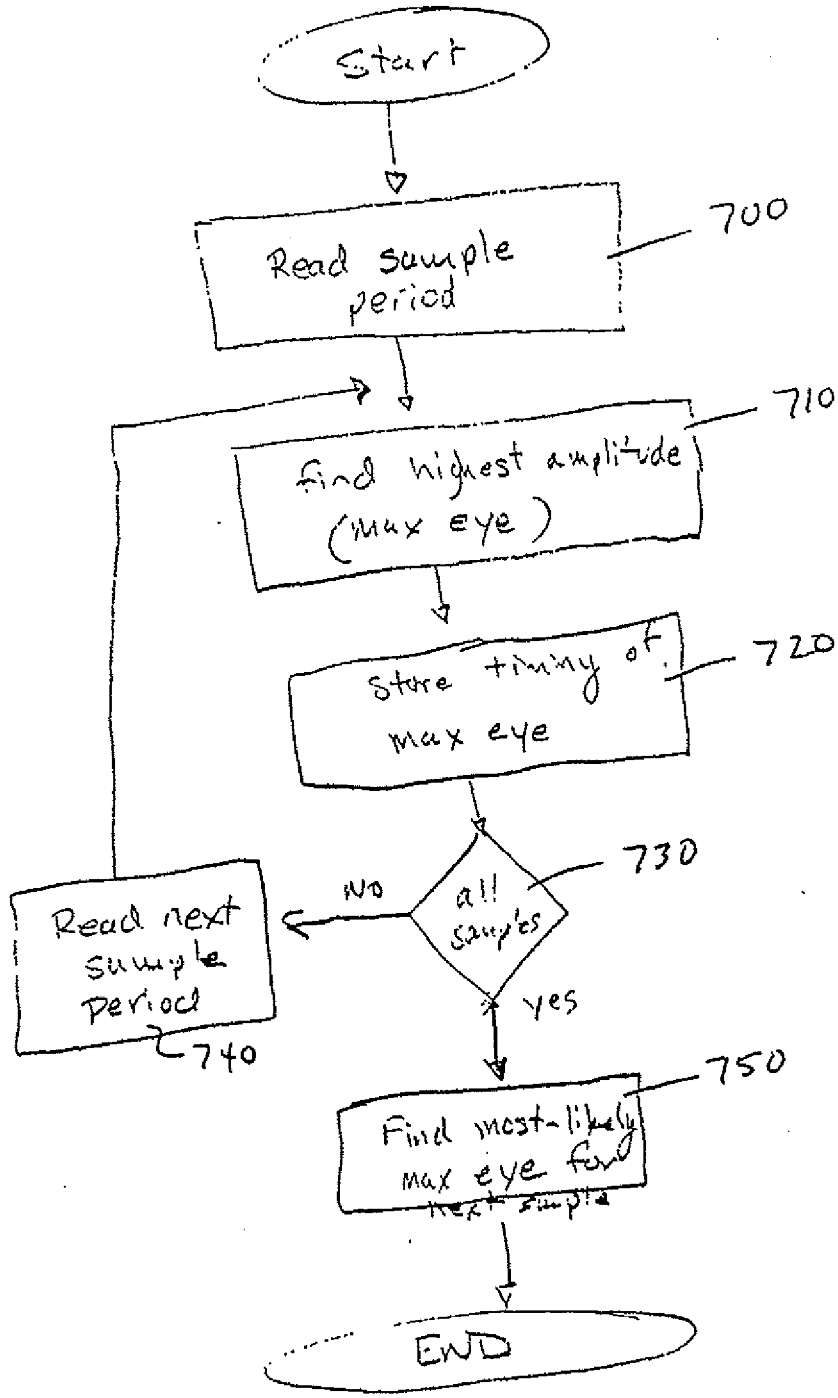

Start
Read sample period
700
find highest amplitude (max eye)
710
Store timing of max eye
720
all samples
730
No
yes
Read next sample period
740
Find most-likely max eye for next sample
750
END

FIG. 7

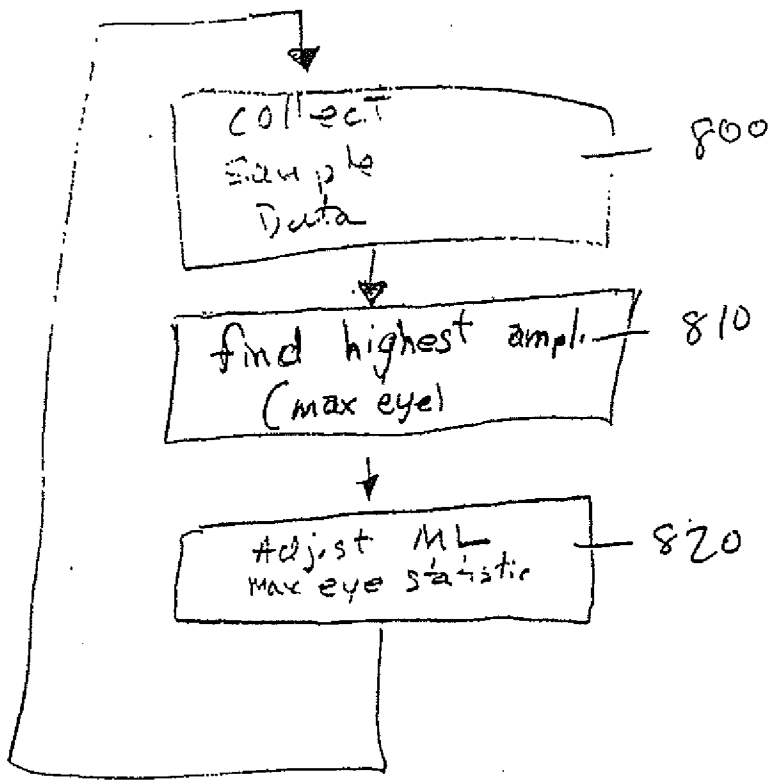

collect
sample
Data
800
find highest ampl.
(max eye)
810
Adjust ML
max eye statistic
820

FIG. 8

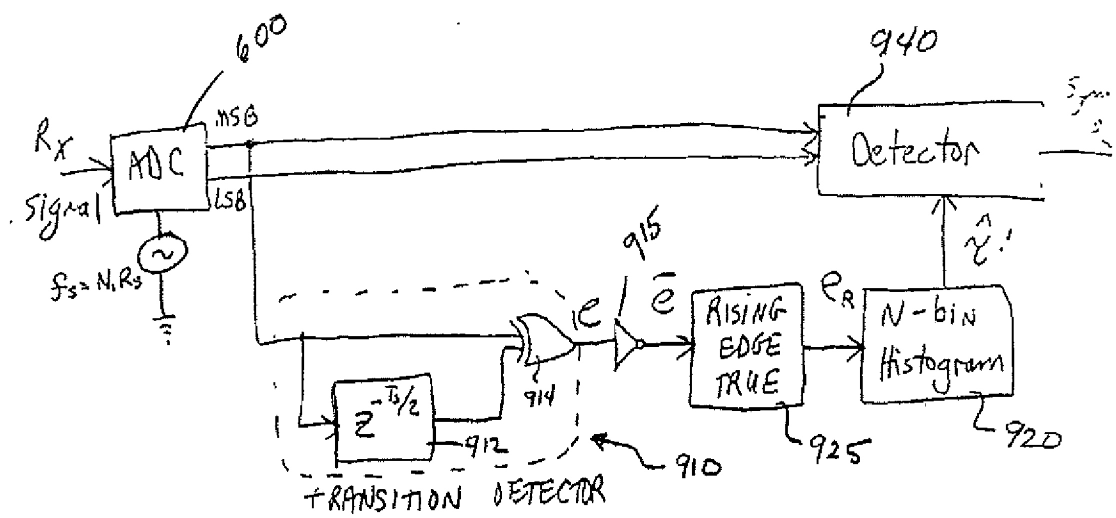

600
940
Rx
Signal
ADC
MSB
LSB
$f_s = N_1 R_s$
Detector
915
e
$\bar{e}$
RISING EDGE TRUE
e_R
N-bin Histogram
$\hat{\tau}$
$z^{-T_s/2}$
914
912
910
925
920
TRANSITION DETECTOR

FIG. 9

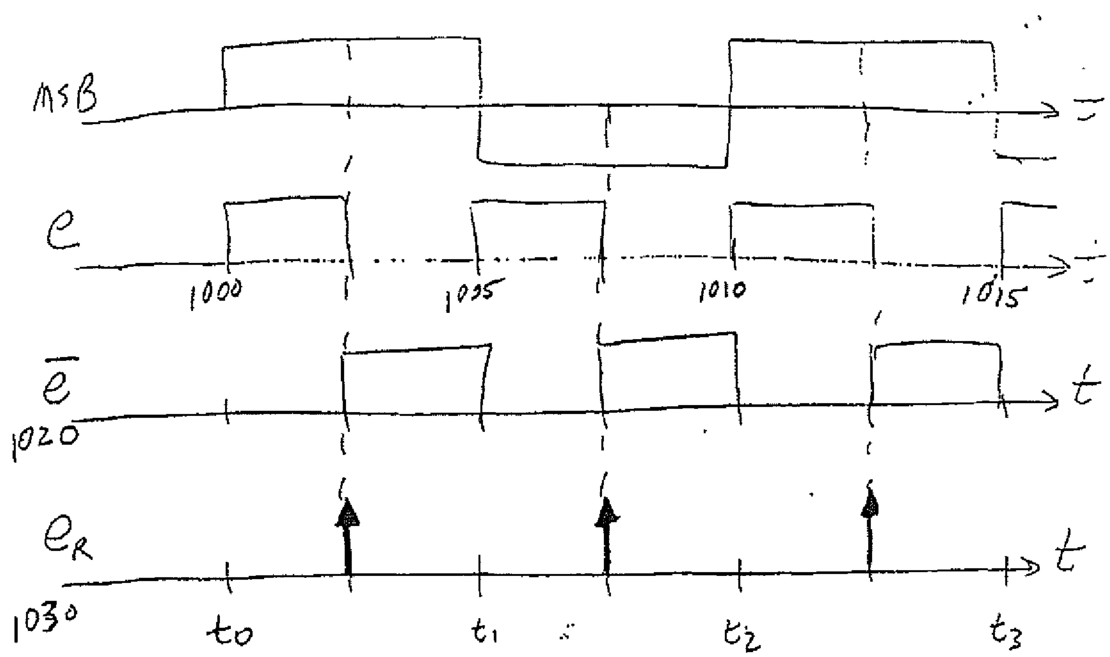


FIG. 10

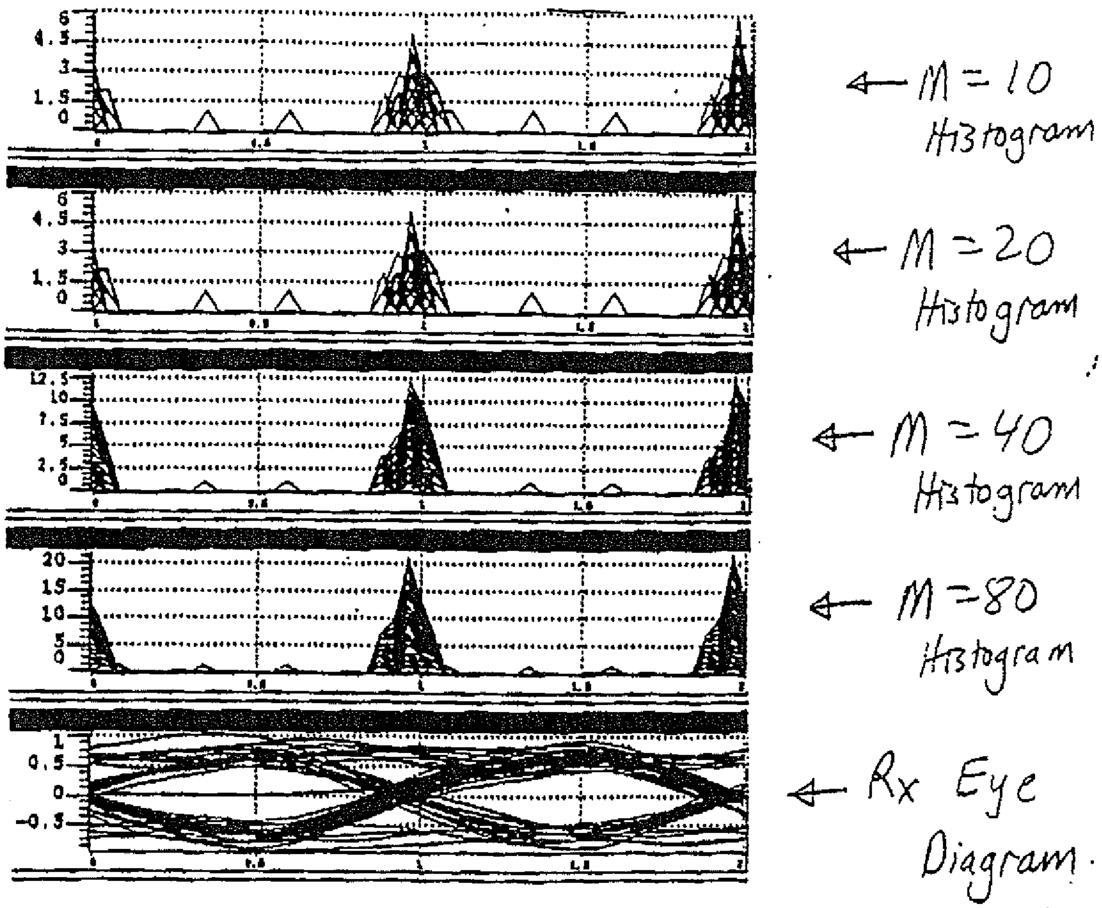

M = 10 Histogram
M = 20 Histogram
M = 40 Histogram
M = 80 Histogram
Rx Eye Diagram.

FIG. 11 A

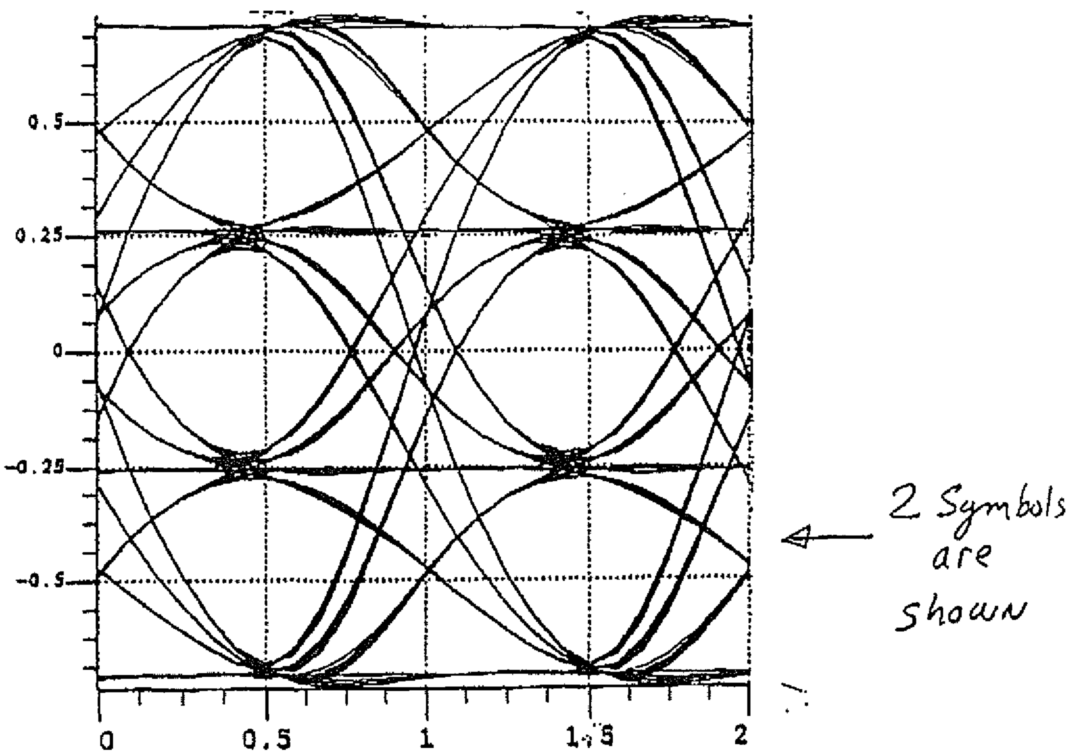


FIG. 11B

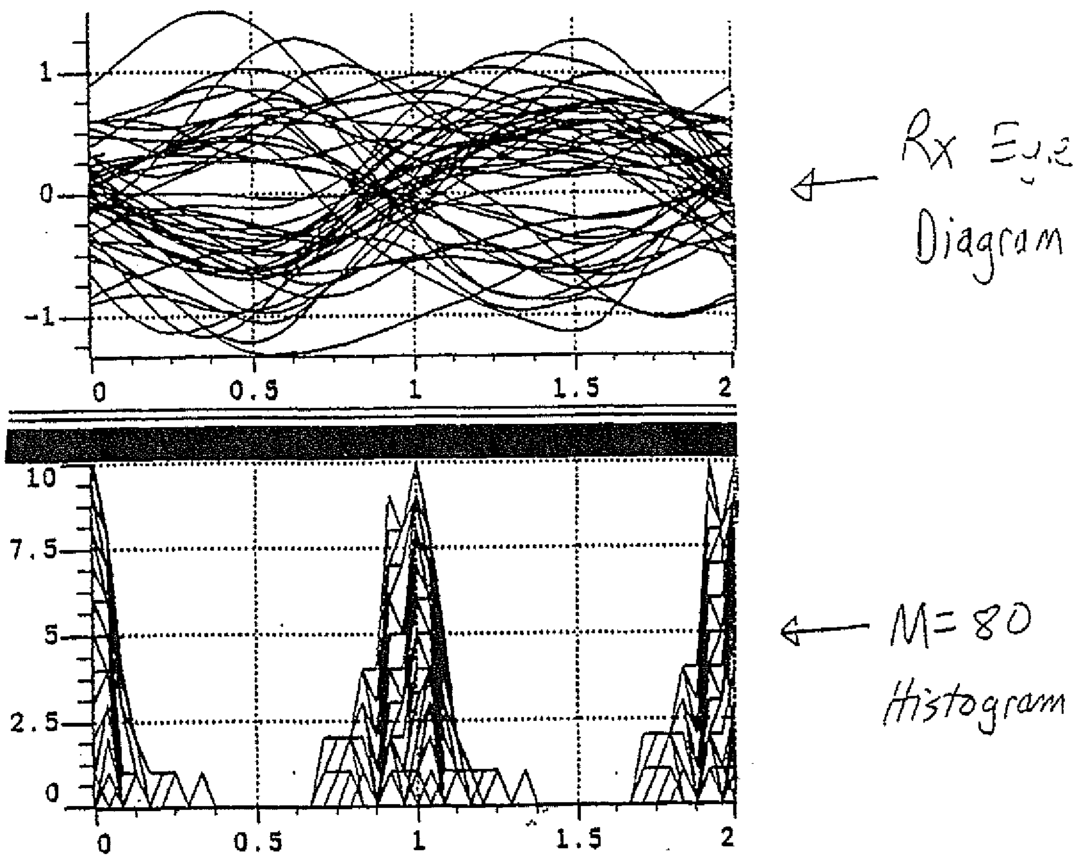


FIG. 12

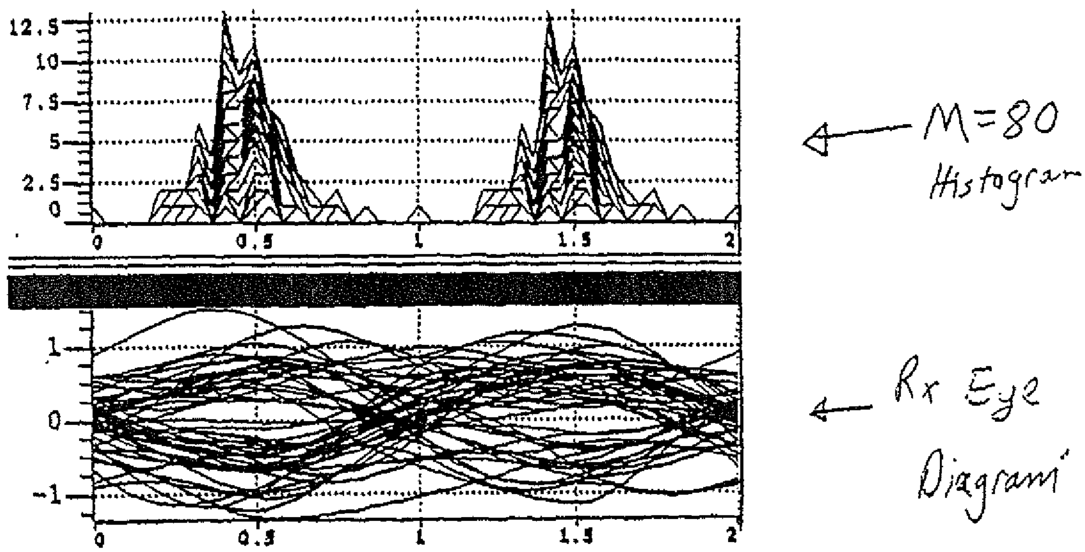

12.5
10
7.5
5
2.5
0
0
0.5
1
1.5
2
M=80
Histogram
1
0
-1
0
0.5
1
1.5
2
Rx Eye
Diagram

FIG. 13

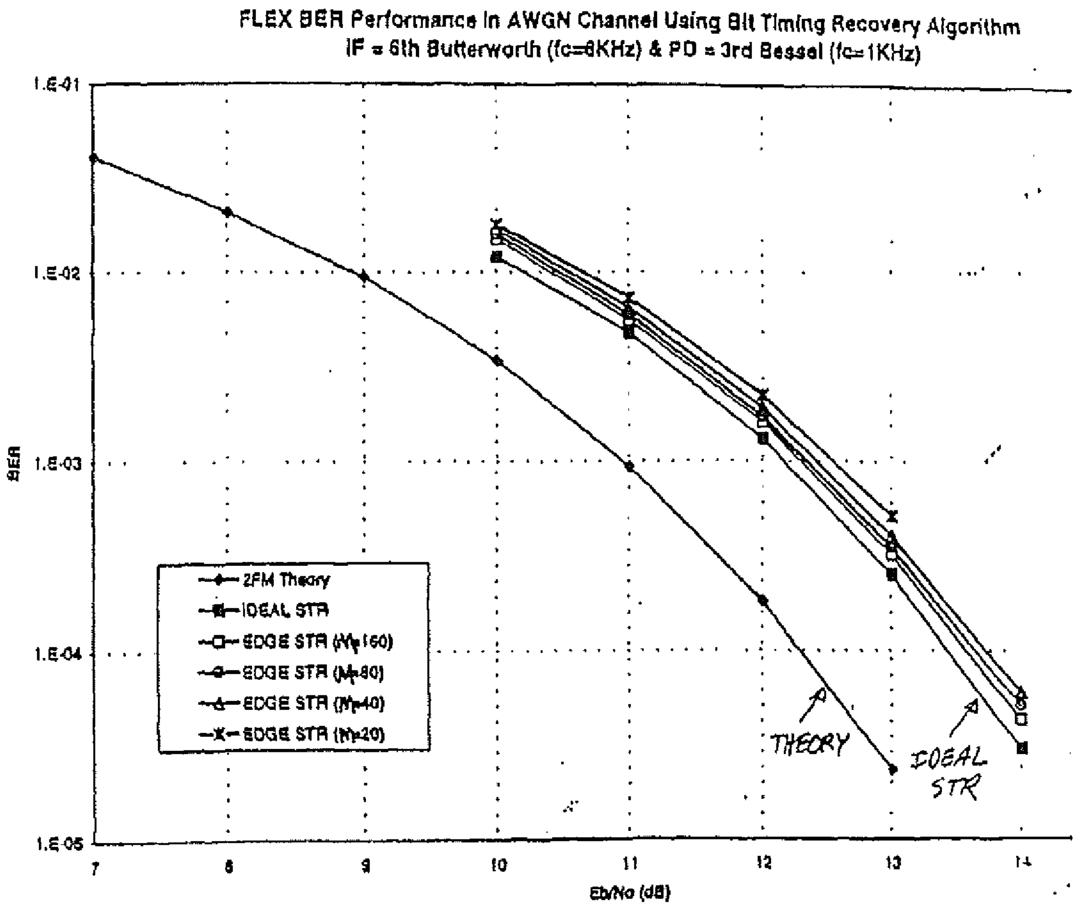

FLEX BER Performance In AWGN Channel Using Bit Timing Recovery Algorithm
IF = 6th Butterworth (fc=6KHz) & PD = 3rd Bessel (fc=1KHz)
BER
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
7
8
9
10
11
12
13
14
Eb/No (dB)
2FM Theory
IDEAL STR
EDGE STR (M=160)
EDGE STR (M=80)
EDGE STR (M=40)
EDGE STR (M=20)
THEORY
IDEAL STR

FIG. 14

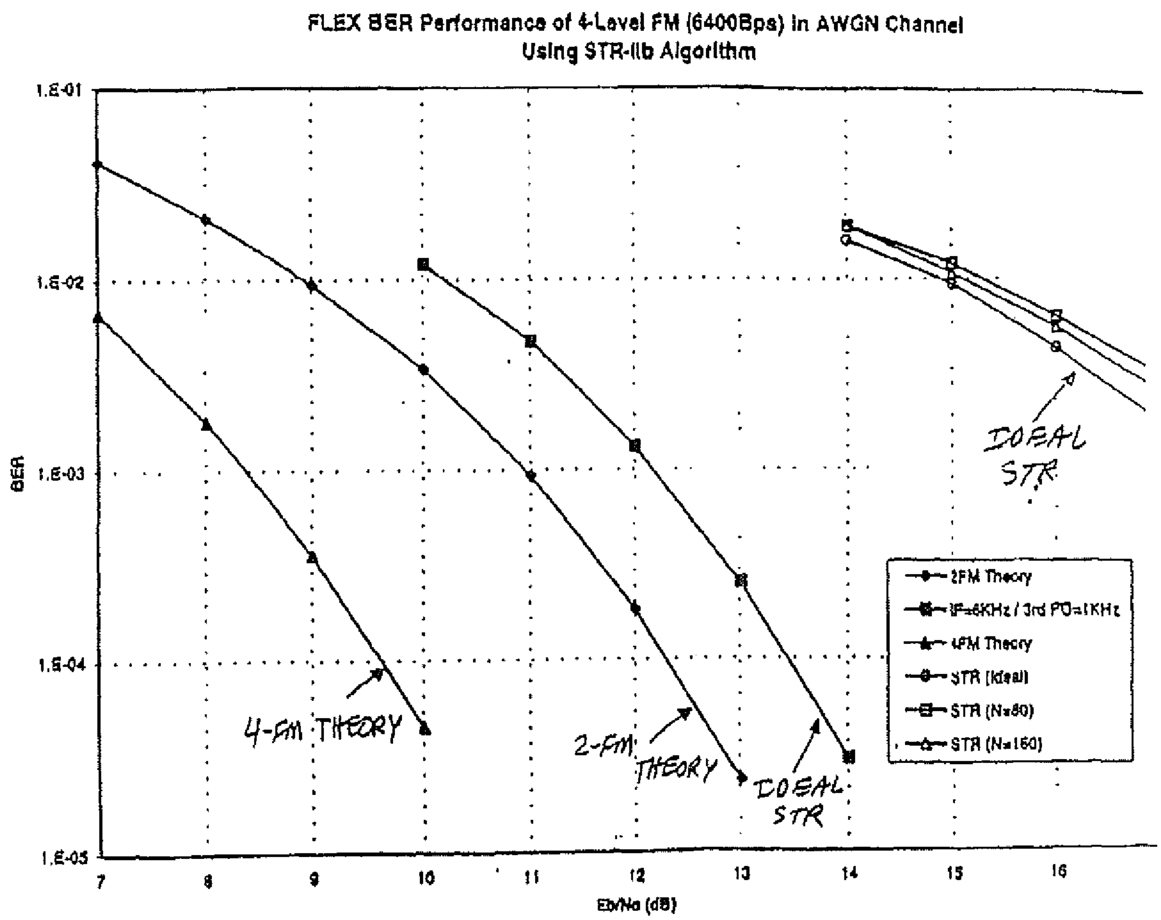

FLEX BER Performance of 4-Level FM (6400Bps) in AWGN Channel
Using STR-IIb Algorithm
BER
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
7
8
9
10
11
12
13
14
15
16
Eb/No (dB)
2FM Theory
IF=6KHz / 3rd PO=1KHz
4FM Theory
STR (Ideal)
STR (N=80)
STR (N=160)
4-FM THEORY
2-FM THEORY
IDEAL STR
IDEAL STR

FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/31128

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H04L 7/00, H04L 25/36, HO4L 27/22, H03D 1/00, H03D 3/24
US CL : 375/355, 375/320, 375/326, 375/348
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 375/355, 375/320, 375/321, 375/326, 375/346, 375/348, 375/371

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPAT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A, P	U.S. 6,314,129 B1 (SUNWOO et al) 06 November 2001. See entire document.	1 - 21
A, P	U.S. 6,154,510 A (COCHRAN et al) 28 November 2000. See entire document	1-21
A	U.S. 6,128,357 A (LU et al) 03 October 2000. See Abstract	1 - 21
A	U.S. 5,966,188 A (PATEL et al) 12 October 1999. See entire document.	1 - 21

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
07 November 2001 (07.11.2001)

Date of mailing of the international search report
26 FEB 2002

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231
Facsimile No. (703)305-3230

Authorized officer
Dung X. Nguen
Karen L. Ward
Telephone No. (703) 305-4892

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